A CAHNERS PUBLICATION
INTERNATIONAL EDITION
MARCH 2, 1989

20 MAR 1989

EDN®

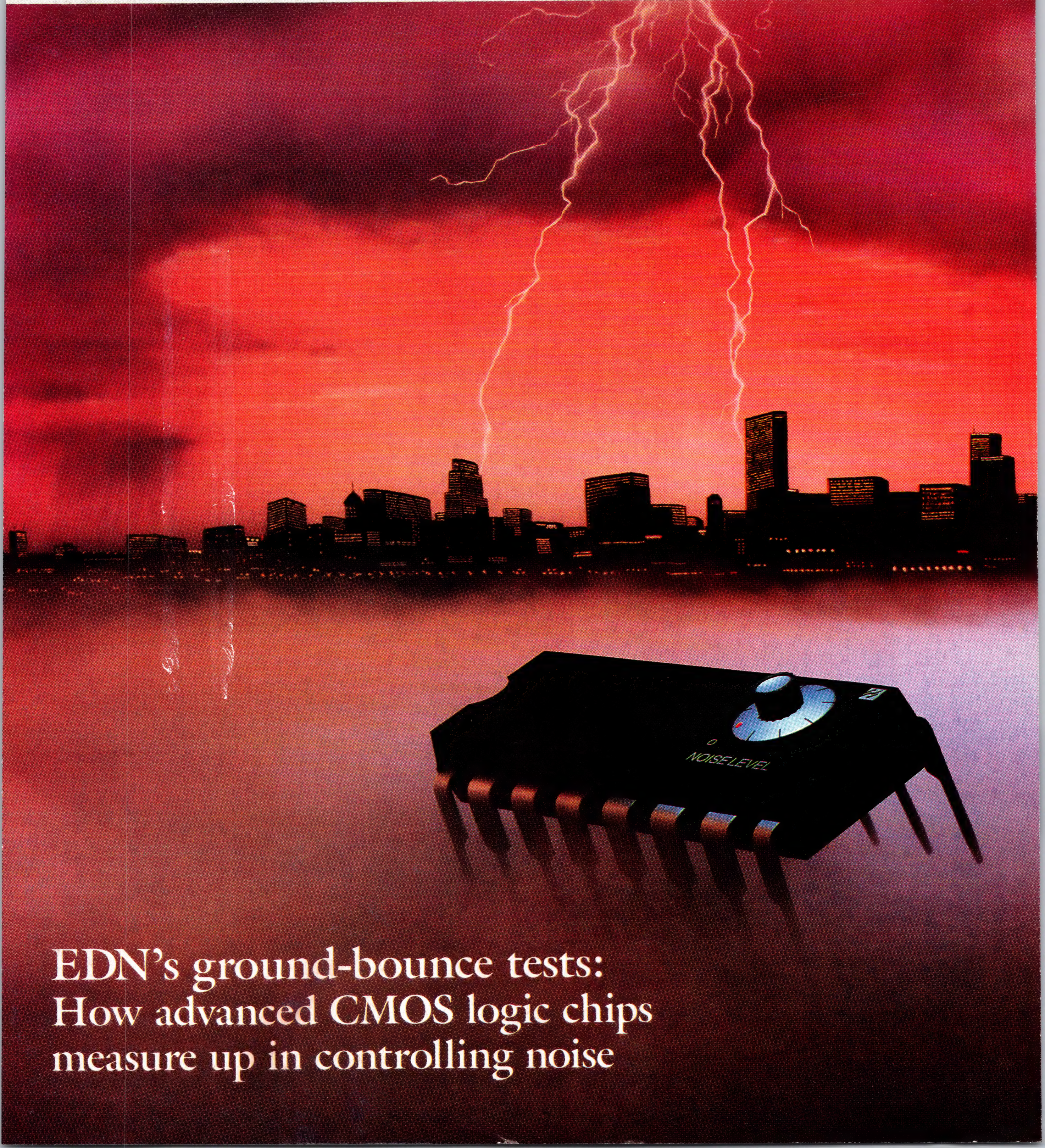
ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Troubleshooting analog circuits—Part 5

Static column decode speeds DRAM access times

Time-measuring instruments break new ground

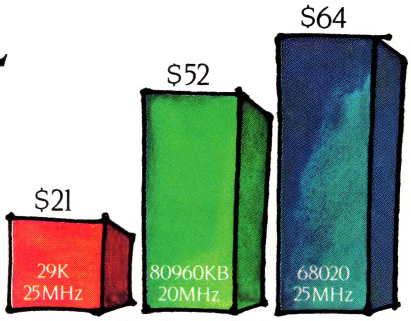
RF/microwave CAE tools



EDN's ground-bounce tests: How advanced CMOS logic chips measure up in controlling noise

simulators. Hardware debug module by Step Engineering. All available from AMD.

Behavioral models from Logic Automation. Real time OS by Ready Systems. Logic analyzer interfaces from HP. And more.



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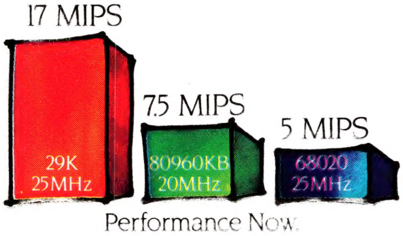

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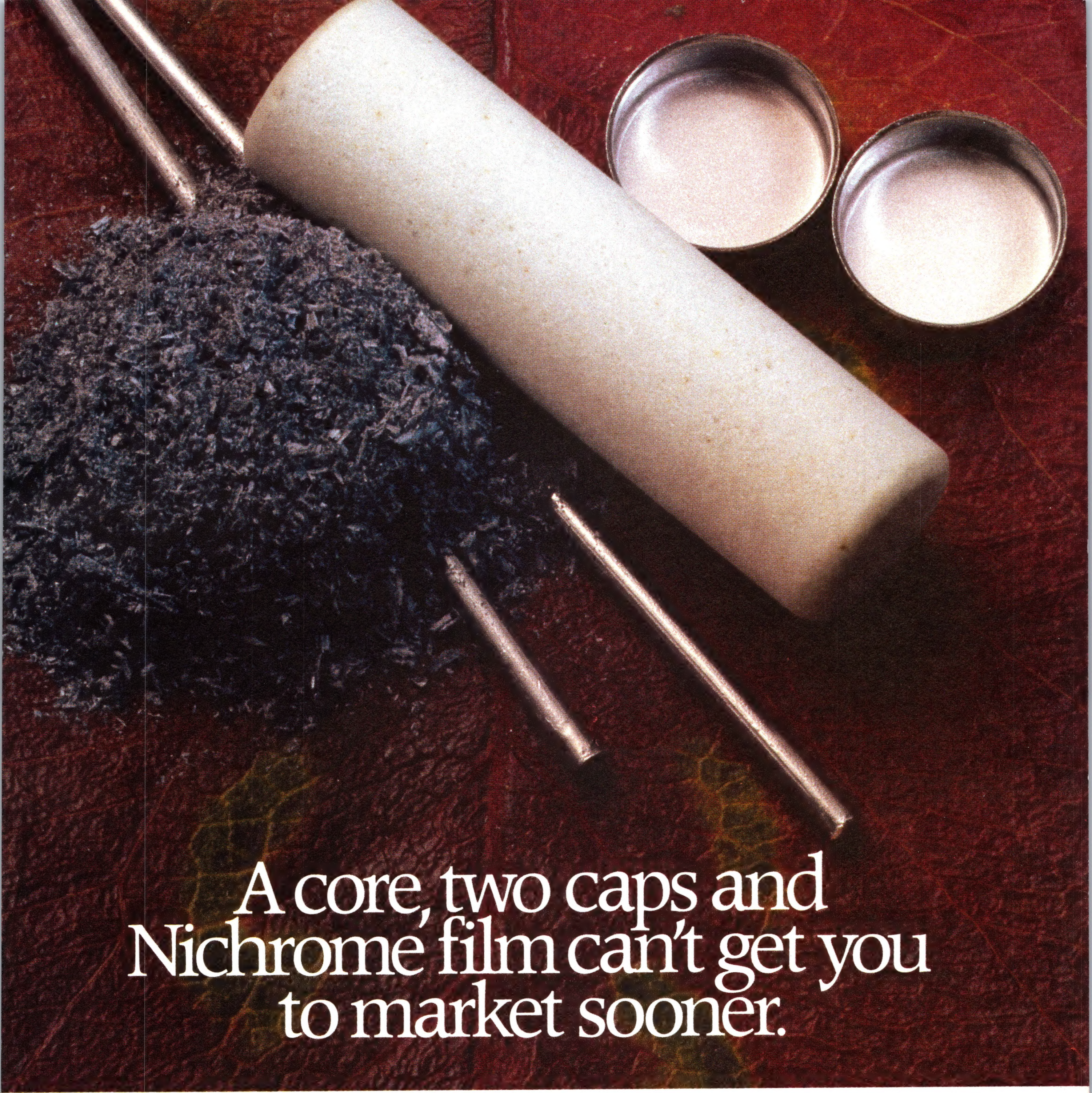
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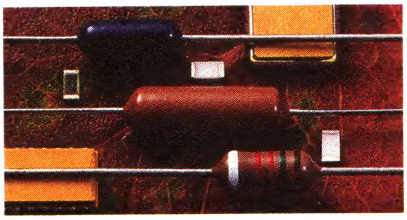

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with new UniLab 8620 analyzer-emulator.

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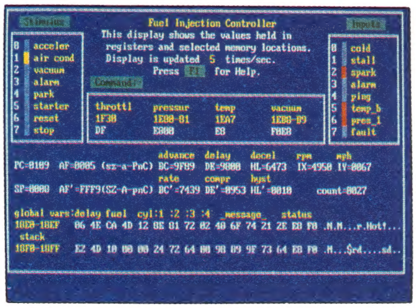
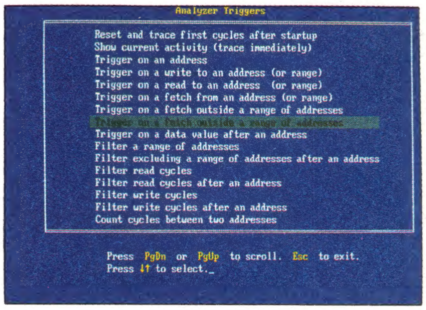


```
Stimulus              Fuel Injection Controller                        Inputs
               This display shows the values held in
0  acceler      registers and selected memory locations.          0  cold
1  air cond     Display is updated  5  times/sec.                 1  stall
2  vacuum                 Press  F1  for Help.                    2  spark
3  alarm       Command:                                           3  alarm
4  park                                                           4  ping
5  starter     throttl     pressur     temp      vacuum            5  temp_b
6  reset       1F30        1E00-01     1EA7      1E00-09           6  pres_1
7  stop        DF          E000        E8        F0E8              7  fault

                         advance  delay    decel    rpm     mph
PC=0109  AF=0005 (sz-a-PnC) BC=9F89  DE=9000  HL=6473  IX=4950 IY=0067
                         rate     compr    hyst
SP=0000  AF'=FFF9(SZ-A-pnC) BC'=7439 DE'=0953 HL'=0010    count=0027

global vars:delay fuel  cyl:1 :2 :3 :4  _message_  status
10E0-10EF   06 4E CA 4D 12 0E 01 72 02 40 6F 74 21 2E E0 F0 .N.M...r.Hot!...
 stack
10F0-10FF   E2 4D 10 00 00 24 72 64 00 90 09 9F 73 64 E0 F0 .M...$rd....sd..
```

InSight Display. InSight blends analyzer-emulator techniques to give you continuous, real time monitoring of key processor functions. And still services user interrupts. It displays changing register contents, I/O lines, ports, user-defined memory windows. With your own labels.



```
                    Analyzer Triggers

        Reset and trace first cycles after startup
        Show current activity (trace immediately)
        Trigger on an address
        Trigger on a write to an address (or range)
        Trigger on a read to an address  (or range)
        Trigger on a fetch from an address (or range)
        Trigger on a fetch outside a range of addresses
        Trigger on a fetch outside a range of addresses
        Trigger on a data value after an address
        Filter a range of addresses
        Filter excluding a range of addresses after an address
        Filter read cycles
        Filter read cycles after an address
        Filter write cycles
        Filter write cycles after an address
        Count cycles between two addresses

          Press  PgDn  or  PgUp  to scroll.  Esc  to exit.
          Press ↓↑ to select._
```

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CIRCLE NO 11

AMERICAN EXPRESS

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absorptive... reflective

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Tough enough to pass stringent MIL-STD-883 tests, useable from dc to 6GHz and smaller than most RF switches, Mini-Circuits' hermetically-sealed (reflective) KSW-2-46 and (absorptive) KSWA-2-46 offer a new, unexplored horizon of applications. Unlike pin diode switches that become ineffective below 1MHz, these GaAs switches can operate down to dc with control voltage as low as -5V, at a blinding 2ns switching speed.

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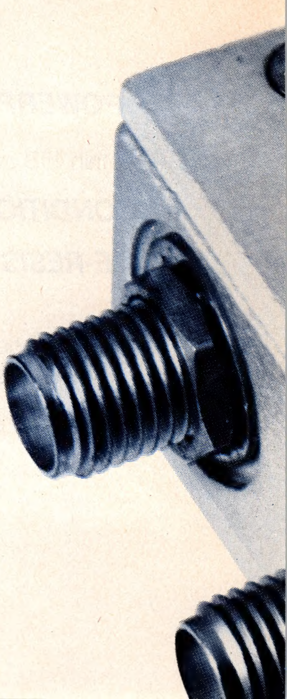
SPECIFICATIONS

Pin Model	**KSW-2-46**		**KSWA-2-46**	
Connector Version	**ZFSW-2-46**		**ZFSWA-2-46**	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec) rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	-8V on, OV off		-8V on, OV off	
OPER/STOR TEMP.	-55° to +125°C		-55° to +125°C	
PRICE (10-24)	**$32.95** **$69.95**		**$48.95** **$79.95**	



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CIRCLE NO 12

EDN Magazine Edition

Volume 34, Number 5

March 2, 1989

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

On the cover: *All logic chips are created noisy, and advanced CMOS logic (ACL) is one of the noisiest logic families. ACL is also difficult to use. To assist you in choosing the best ACL chip for your design, EDN conducted ground-bounce tests on chips from five major ACL manufacturers. Turn to pg 88 for the results. (Photo courtesy National Semiconductor Corp)*

SPECIAL REPORT

EDN's advanced CMOS logic ground-bounce tests 88

For years, manufacturers of advanced CMOS logic (ACL) chips have squabbled over solutions to the chips' inherent noise problem. Now that ACL chips are widely available in OEM quantities, EDN investigates the issue by running its own ground-bounce tests on chips from five major ACL manufacturers.—*David Shear, Regional Editor*

DESIGN FEATURES

Static column decode speeds up DRAM access time 125

Static column decode can't expedite μP throughput as well as cache memory can, but it is an inexpensive way to improve the performance of conventional 1M-bit dynamic-RAM (DRAM) chips.—*Robert Breuninger, Loren Schiele, Joshua Peprah, Texas Instruments Inc*

A state machine handles back-end processing for clustered networks 141

Often, systems designers focus on the front-end protocols in network communications. But when a data network interfaces with many multiplexed devices through a gateway, the heavy back-end traffic can cripple a μP. A state machine can assume most of these back-end communication tasks.—*Brian Bennett, McDonnell Douglas Electronic Systems Co*

Troubleshooting analog circuits—Part 5 159

In addition to your choice of components, the materials you use to assemble your circuit will have an impact on how well it performs. This article, part 5 of a 5-part series on troubleshooting passive components, covers what you need to know to solve the occasional problems caused by pc boards, solder, connectors, wire, and cable. Also covered is pc-board layout.—*Robert A Pease, National Semiconductor Corp*

Continued on page 7

EDN®(ISSN 0012-7515) is published 49 times a year (biweekly with 2 additional issues a month, except for February, which has 3 additional issues and July and December which have 1 additional issue) by Cahners Publishing Company, A Division of Reed Publishing USA, 275 Washington Street, Newton, MA 02158-1630. Terrence M McDermott, President; Frank Sibley, Electronics/ Computer Group Vice President; Jerry D Neth, Vice President/Publishing Operations; J J Walsh, Financial Vice President/Magazine Division; Thomas J Dellamaria, Vice President/Production and Manufacturing. Circulation records are maintained at Cahners Publishing Company, 44 Cook Street, Denver, CO 80206-5800. Telephone: (303) 388-4511. Second-class postage paid at Denver, CO 80206-5800 and additional mailing offices. POSTMASTER: Send address corrections to EDN® at the Denver address. EDN® copyright 1989 by Reed Publishing USA; Saul Goldweitz, Chairman; Ronald G Segel, President and Chief Executive Officer; Robert L Krakoff, Executive Vice President; William M Platt, Senior Vice President. Annual subscription rates for nonqualified people: USA, $105/year; Canada/Mexico, $125/year; Europe air mail, $150/year; all other nations, $150/year for surface mail and $230/year for air mail. Single copies are available for $10. Please address all subscription mail to Eric Schmierer, 44 Cook Street, Denver, CO 80206-5800.

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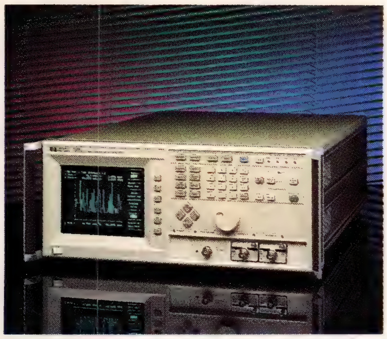

***Time measurement** is a mature market, but don't assume that all recent products incorporate only incremental improvements (pg 47).*

TECHNOLOGY UPDATE

Time-measurement instruments: A mature industry returns to innovation 47

HP dominates the time-measurement market and has earned a reputation for sound design, quality construction, and excellent postsale support. Nonetheless, if you limit yourself to HP products, you can easily miss some of the reasonably priced, well-designed, and well-built instruments that other manufacturers offer. Some products actually break new ground.—*Dan Strassberg, Associate Editor*

RF/microwave CAE tools: Software programs ease circuit designer's task 63

In choosing a CAE software package, you need to consider a program's capabilities in terms of your specific application requirements and—of equal importance—the particular computer on which the software runs. Most of the available RF/microwave programs run on IBM PCs, PC/XTs, PC/ATs, and compatibles. Several programs are available that support the Apple II and the Macintosh. —*Dave Pryce, Associate Editor*

PRODUCT UPDATE

ECL-compatible PLDs 86

DESIGN IDEAS

PLD implements programmable delay 171
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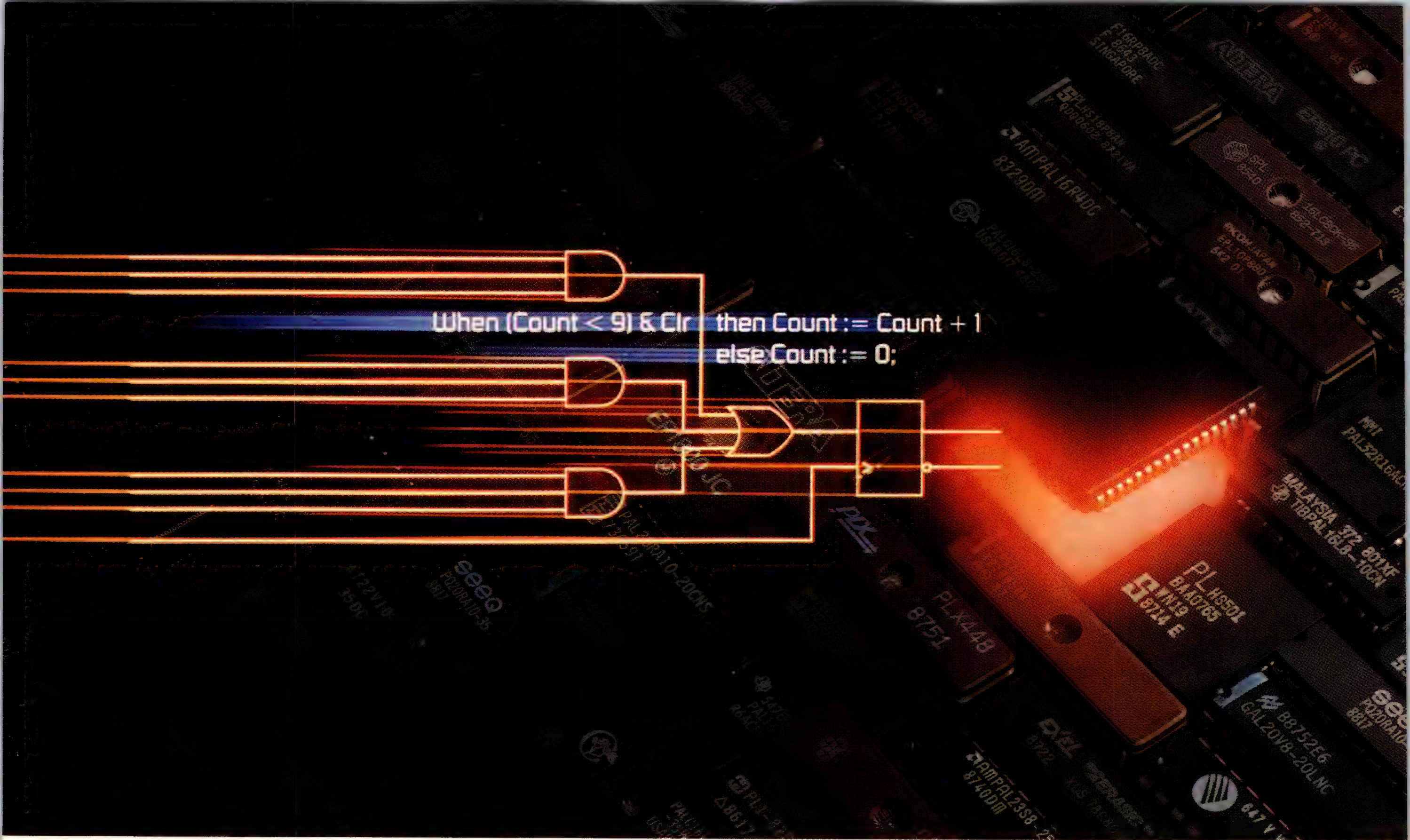

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March 2, 1989

EDITORIAL 45

Coordinating US research and development work would uncover our strengths and weaknesses and help us spend our R&D money wisely.

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Private developer vs federal government: Retaining software rights requires vigilance.—*Stephen T Owen*

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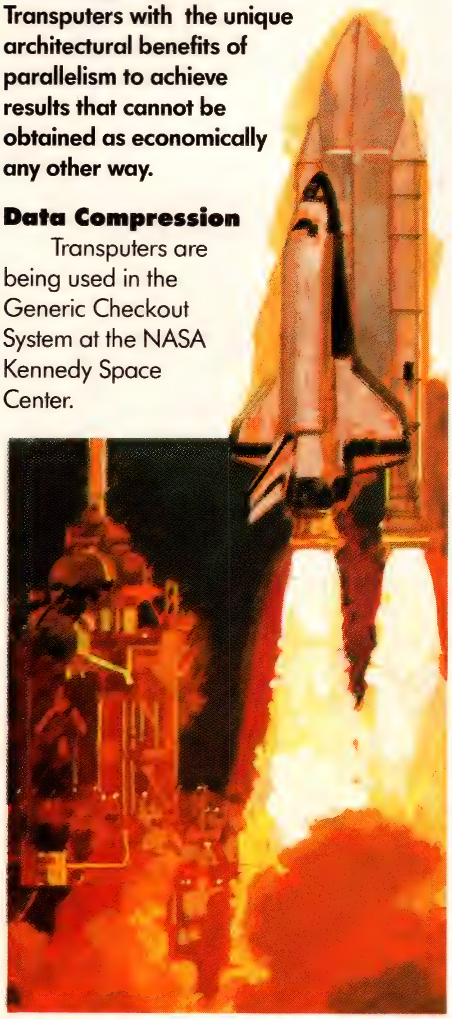
“OK...SO THE TRAN BUT WHAT ABOUT R

They're everywhere. Worldwide over a thousand Transputer designs are in today's marketplace or are entering production. Some belong to Fortune 500 companies committed to using Transputers to build their next-generation products.

Although Transputer applications are diverse, the theme for each is the same – combining the power of individual Transputers with the unique architectural benefits of parallelism to achieve results that cannot be obtained as economically any other way.



Data Compression

Transputers are being used in the Generic Checkout System at the NASA Kennedy Space Center.

They are embedded within VME based front-end Data Acquisition Modules to provide data filtering for the system.

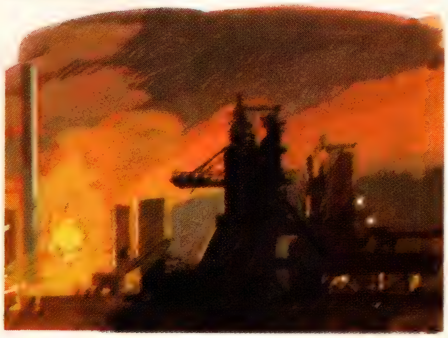
These modules pre-process data for a network of Unix based workstations that provide real-time control and monitoring of ground and flight equipment, like that used by the Space Shuttle. Only Transputers offered the degree of parallelism needed for this application.

Medical Imaging

University College London is using the parallel processing power of Transputers to convert CAT, NMR and laser scans into rotating 3-D images. These facial, skeletal, and soft-tissue images provide accurate computerized measurements to assist doctors with each step of an operation, and are also used by plastic surgeons to 'rehearse' operations for reconstruction.

Data Collection

British Steel is implementing an intelligent system that is designed to dramatically cut its multimillion dollar annual energy costs. It is built around T800 floating point microprocessors which process information from a highly complex data gathering system. These Transputers operate in parallel, condensing enormous amounts of data into information which helps energy management decide how to respond to a plant's changing demands for different fuels.



Data Transmission

Kokusai Denshin Denwa (KDD), the Japanese international telecommunications company, has developed an image-processing video telephone using Transputers to manipulate and condense images for transmission over telephone links.

This image communications system uses 32 Transputers operating in parallel for ultrafast image processing. It can be connected to PC's to transmit images over telephone lines, function as a video phone, or be programmed to match the specifications of other receiving equipment, such as facsimile machines and TV monitors.

Space

The European Space Agency is using Transputers to build a light-weight, radiation-tolerant, on-board computer for spacecraft. Programs which utilize Transputers in scientific computing and spacecraft control applications are also being developed in the U.S.

Transputers are manufactured on epitaxial silicon and have been shown to withstand aggressive tactical radiation levels.

SPUTER’S TERRIFIC, EAL APPLICATIONS?”

Flight Simulation

British Aerospace have used Transputers to develop a low-cost flight simulator comprising a flat world, ground-grid, buildings, trees and mountains – with an optional Head-up display. Future enhancements will include the addition of undulating terrain and a single or triple window display option.

American companies are also using Transputers to build high-performance flight simulators more cheaply. One U.S. manufacturer utilizes over one thousand T800 processors per system.

3-D Rendering

Pixar in the US has developed a Transputer-based rendering system which quickly renders photorealistic images from 3-D models. The system consists of Transputer boards for VME and AT-bus systems optimized to run Pixar's sophisticated rendering software.

The system holds great promise for such applications as architecture, automobile styling, package design, simulation as well as animation. Pixar's recent computer generated film 'Tin Toy' could not have been done without using this Transputer-based accelerator.

System Control

As the number of Transputers in a system design are increased, a proportional increase in performance can be achieved.

In West Germany, Parsytec GmbH is using this principle in their Megaframe Superclusters. Superclusters represent a complete series of reconfigurable industrial control boards as used in the automotive industry, which exploit the Transputer's parallel processing capability.

The basic Model 64, built with T800's, has a performance of 640 MIPS and 96 MFLOPS. The Model 256 comprises four Model 64 cabinets connected by cables and provides 2,560 MIPS and 384 MFLOPS.

Parsytec believes there is no limit to the size Superclusters can grow to. Two Model 256s can be combined easily to realize twice the raw performance of one system.

Robotics

Transputers are ideally suited for robotics applications because their special on-chip links make communication between control centers naturally easy. They are often used in the central control area for dumb robots, in multi-jointed robots, and in machine vision systems.

At the Houston Space Center, NASA and Lockheed are using Transputers in the development of an intelligent, self-manoeuvering, voice-controlled robot named EVA Retriever. EVAR is being built to investigate the autonomous retrieval of objects and astronauts that become detached from the Space Station.

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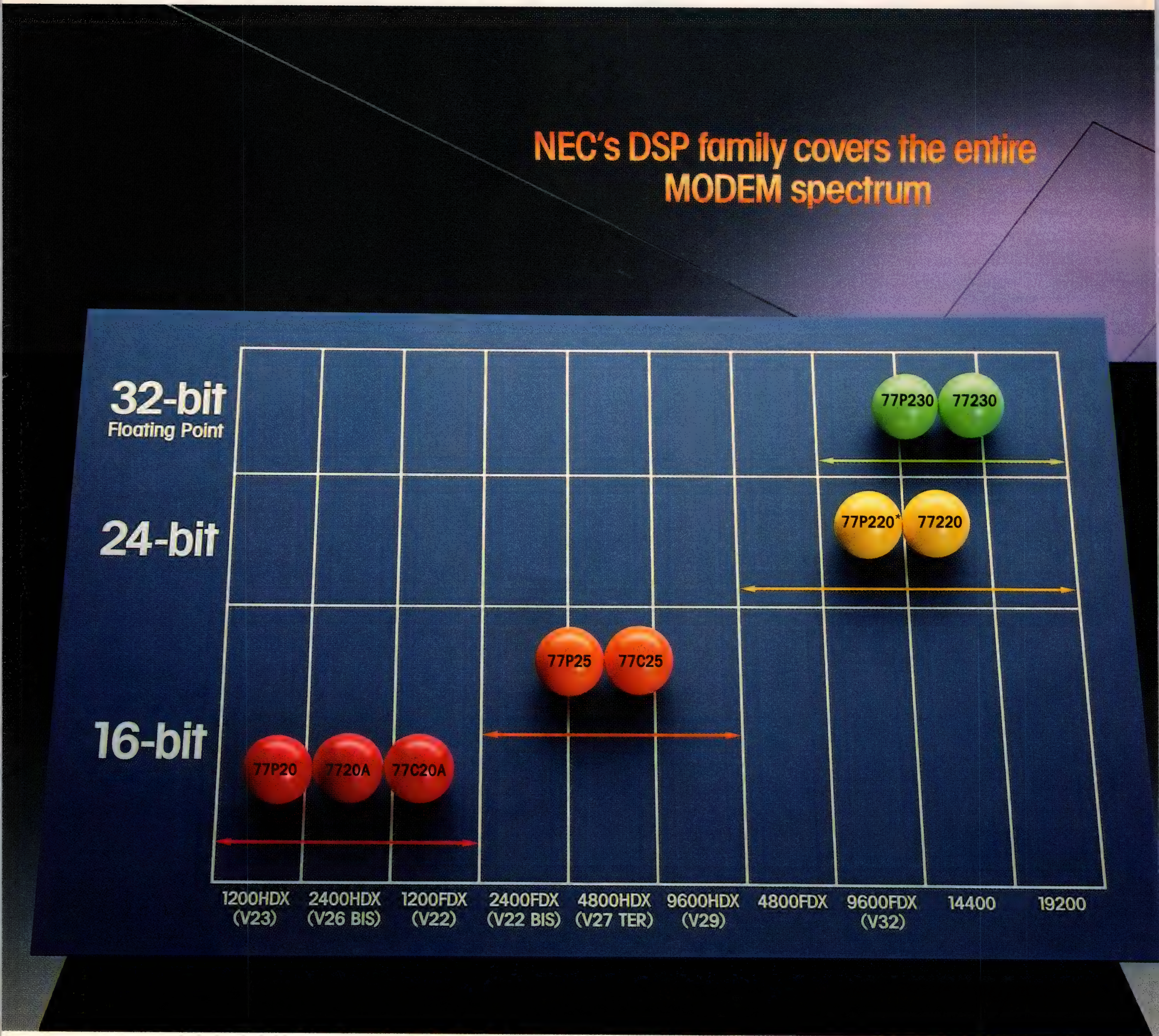
CIRCLE NO 15

The 16-bit sensation from



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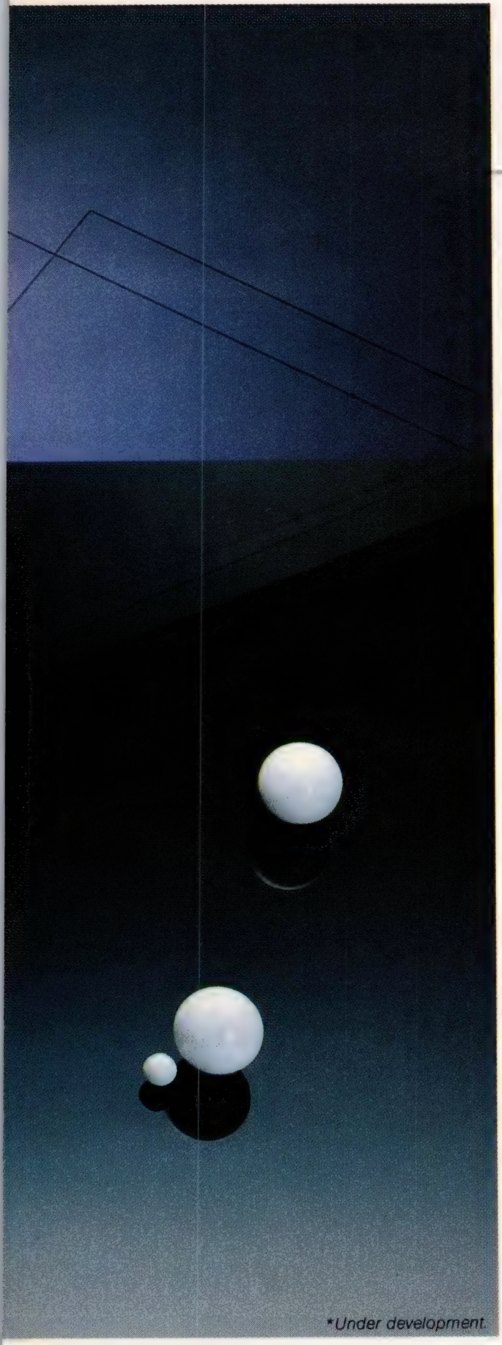

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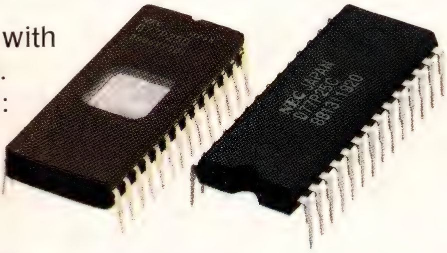
The 77C25 comes in a 28-pin DIP or 44-pin PLCC. It's pin- and software-compatible at the source level with the 77C20A. Development tools are available off the shelf.

NEC also offers a choice of programmable versions:

- ☐ EPROM in CerDIP with window: 77P25D.
- ☐ OTP in plastic DIP: 77P25C.
- ☐ OTP in PLCC: 77P25L.



In addition, we supply socket adaptors (PA-77P25C/PA-77P25L) for programmers.

Whatever your modem design calls for, NEC's DSP family has the answers. From 1,200 to 19,200bps and everywhere in between, the DSP powerhouse has you covered. Call us on it, today.

CIRCLE NO 16

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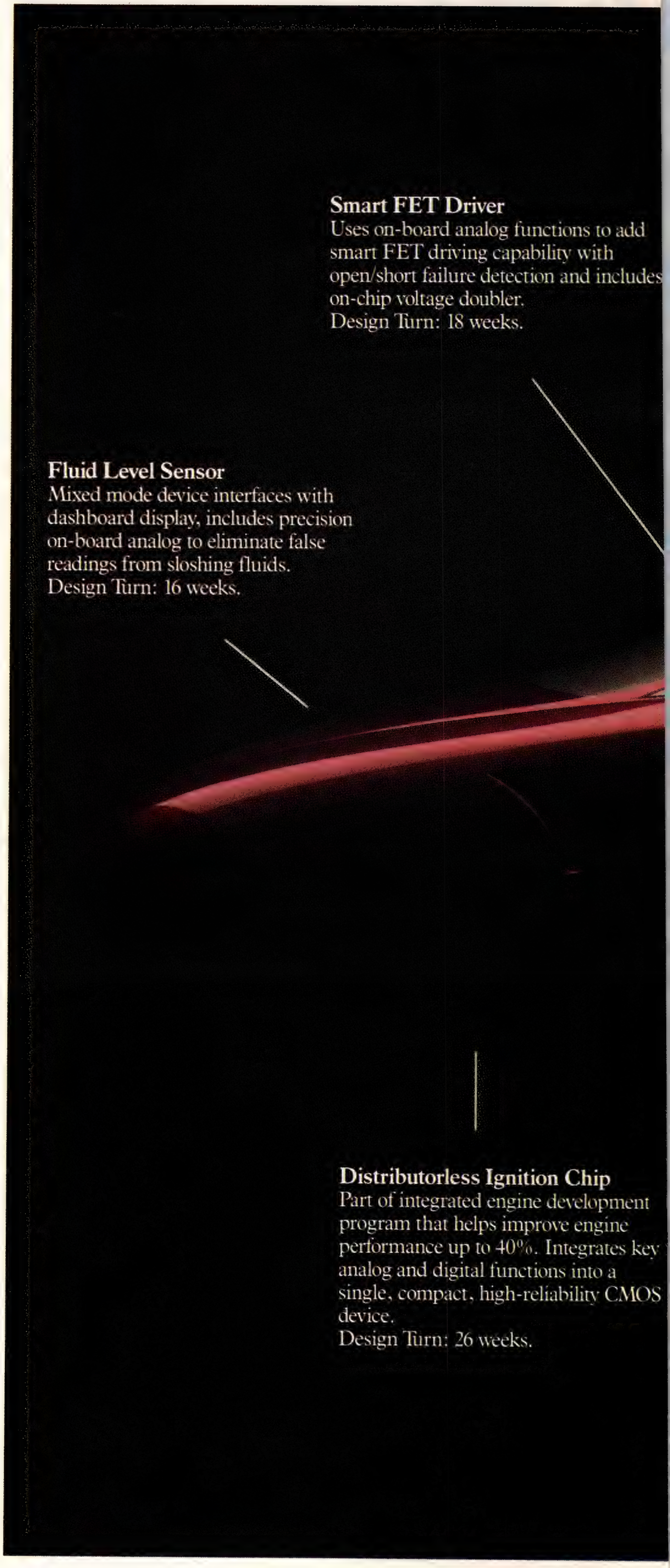
CIRCLE NO 17

Creating value



Smart FET Driver
Uses on-board analog functions to add smart FET driving capability with open/short failure detection and includes on-chip voltage doubler.
Design Turn: 18 weeks.

Fluid Level Sensor
Mixed mode device interfaces with dashboard display, includes precision on-board analog to eliminate false readings from sloshing fluids.
Design Turn: 16 weeks.

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Part of integrated engine development program that helps improve engine performance up to 40%. Integrates key analog and digital functions into a single, compact, high-reliability CMOS device.
Design Turn: 26 weeks.

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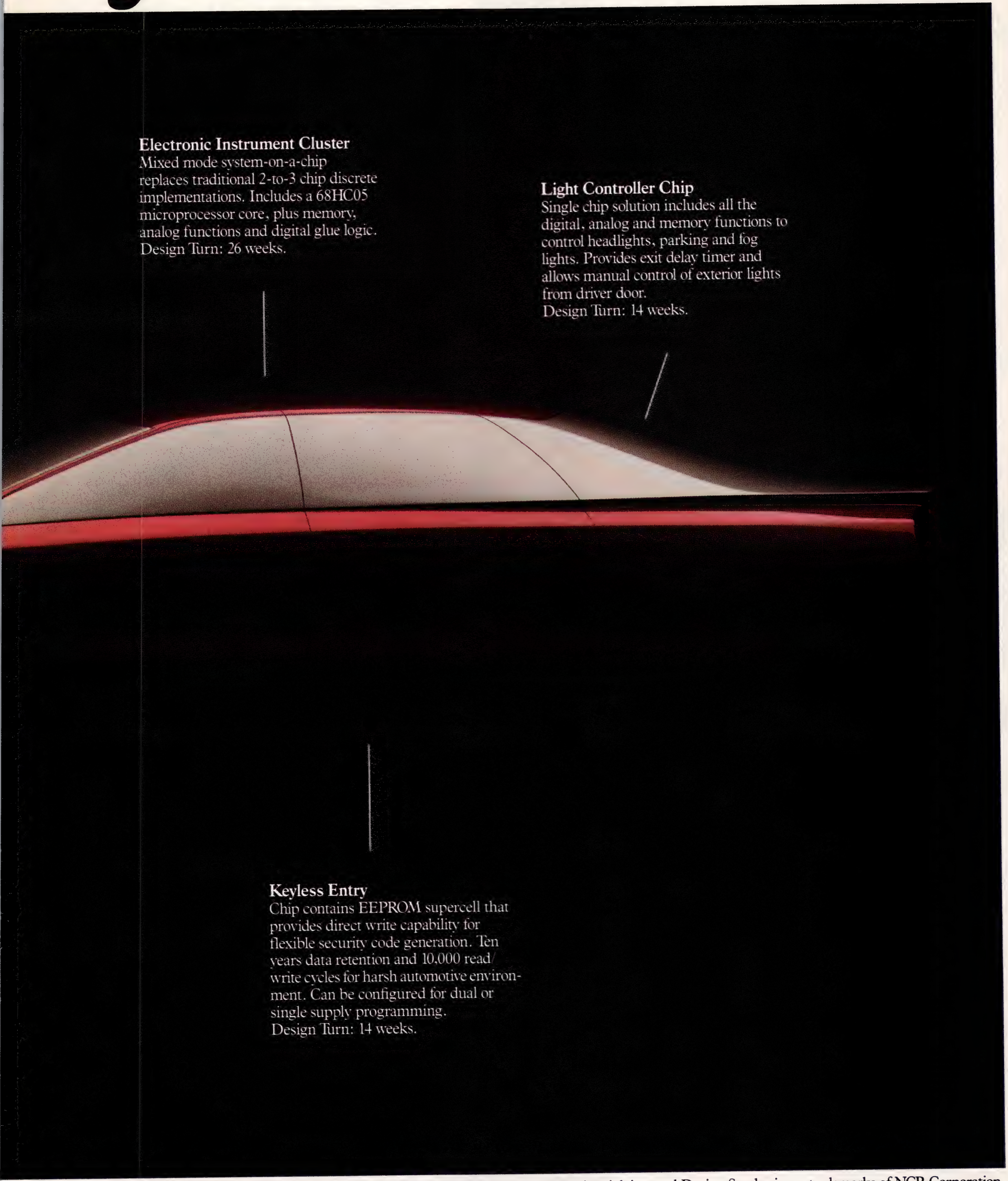

Electronic Instrument Cluster
Mixed mode system-on-a-chip replaces traditional 2-to-3 chip discrete implementations. Includes a 68HC05 microprocessor core, plus memory, analog functions and digital glue logic.
Design Turn: 26 weeks.

Light Controller Chip
Single chip solution includes all the digital, analog and memory functions to control headlights, parking and fog lights. Provides exit delay timer and allows manual control of exterior lights from driver door.
Design Turn: 14 weeks.

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Chip contains EEPROM supercell that provides direct write capability for flexible security code generation. Ten years data retention and 10,000 read/write cycles for harsh automotive environment. Can be configured for dual or single supply programming.
Design Turn: 14 weeks.

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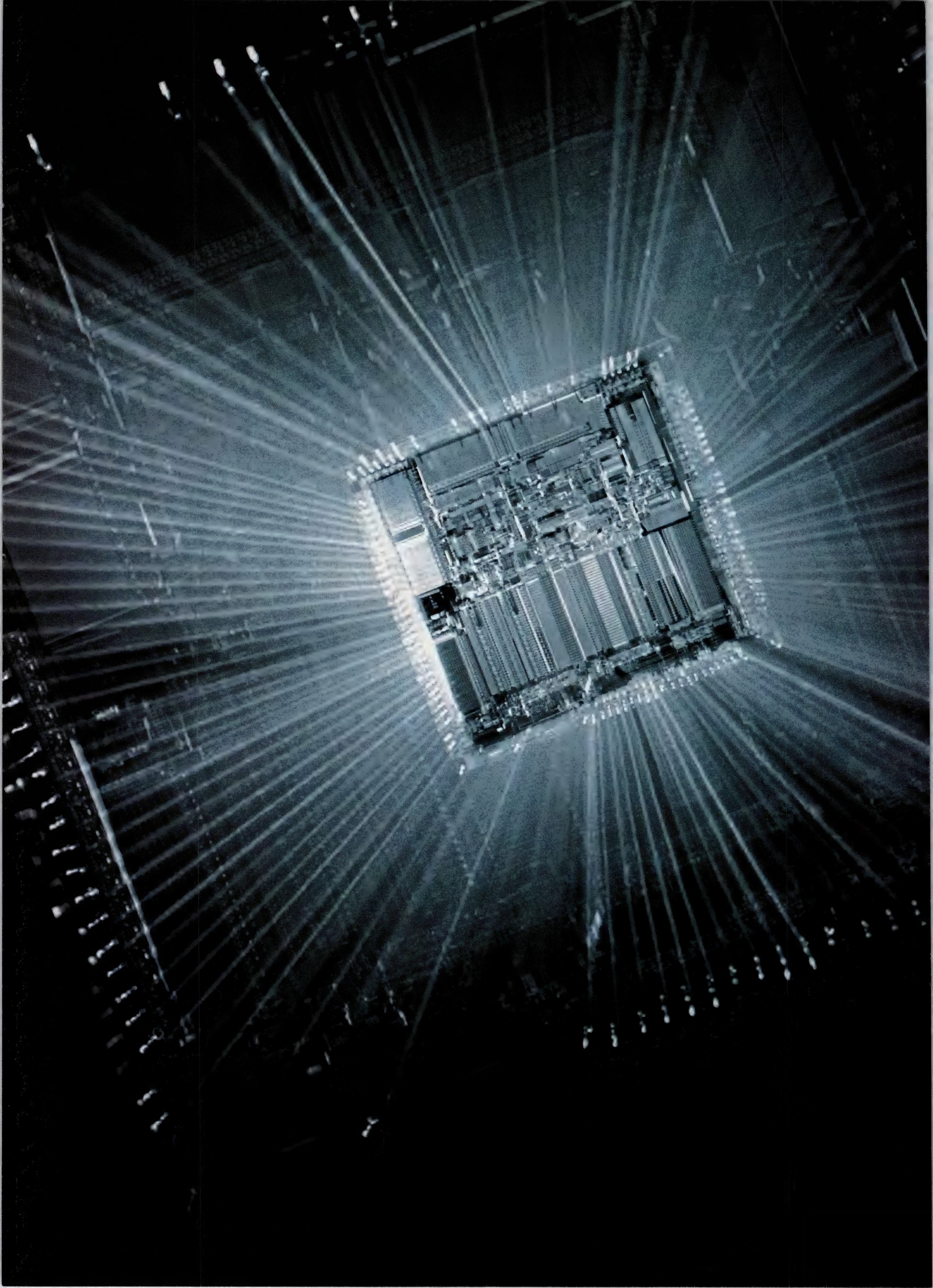

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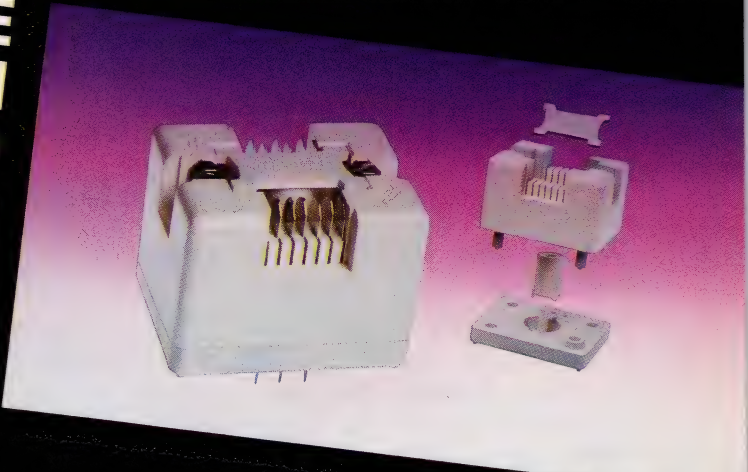

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TECH TOPICS

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CIRCLE NO 21

WAVETEK

NEWS BREAKS

EDITED BY JOANNE DE OLIVEIRA

SINGLE CHIP INTEGRATES CACHE-CONTROLLER AND MMU FUNCTIONS

The CY7C604 CMU (cache and memory unit) from Cypress Semiconductor (San Jose, CA, (408) 943-2600) integrates the functions of a cache controller with those of a memory-management unit (MMU) for the company's 32-bit CY7C601 SPARC µP. The MMU section accepts 32-bit virtual addresses and generates 36-bit physical addresses organized into 4k-byte pages. Address translation takes place by means of a 3-level table that is directly supported by on-chip table-walking circuitry. Access protection takes place at the page level. A 64-entry translation look-aside buffer (TLB) performs the address mapping and holds the context and protection bits. If you need more than 64 TLB registers for your application, you can use as many as 16 CMUs in parallel for one µP. You can lock entries into the TLB to achieve deterministic response times for critical sections of code.

The CMU's cache controller manages a cache RAM as large as 64k bytes by means of 2048 cache-tag entries. You can add extra CMUs in parallel to extend the maximum cache-RAM size to 256k bytes. The company also offers the CY7C157, a 20-nsec, 16k × 16-bit static RAM for use as the cache memory. The cache controller operates in either write-through or copy-back mode. Both the MMU and the cache sections support 4096 contexts. The CY7C604 CMU costs $719.94 (100); the CY7C157 RAM costs $105.60 (100). Samples of both devices will be available in the second quarter of 1989. In the third quarter, the company will introduce the CY7C605 CMU-MP, which is software compatible with the CY7C604, but incorporates enhancements for multiprocessing applications.—Steven H Leibson

COMPANIES WILL MARKET SIMULATOR INTERFACE JOINTLY

Under the terms of an agreement between Gateway Design Automation Corp (Lowell, MA, (508) 458-1900) and Meta-Software Inc (Campbell, CA, (408) 371-5100), the two companies are developing an interface between the Verilog-XL digital-logic simulator and the HSPICE analog-circuit simulator. The interface will enable you to simulate analog subsystems in their digital systems context and to execute HSPICE within the Verilog kernel. The Verilog/HSPICE interface will be available from both companies in the third quarter of 1989.—Michael C Markowitz

1.5-µM ASIC LIBRARY ADDS 8200 SERIES PERIPHERAL CELLS

NCR Microelectronics Div (Fort Collins, CO, (800) 334-5454) is adding macrocells that perform the functions of several 8200 Series peripheral chips to its 1.5-µm ASIC library. The macrocells will perform the functions of the 8237A DMA controller, 8250A/16450 UART, 8254 counter/timer, 8259 interrupt controller, 82288 bus controller, and 82284 clock generator. The company has added built-in testability circuitry to the 8237A macrocell and has developed test patterns for the other cells. The functions are already available in the company's 2-µm cell library. They'll be available in the 1.5-µm library by the end of June.—Steven H Leibson

FAST CMOS STATIC RAMS OPERATE AT 3.3V

Performance Semiconductor (Sunnyvale, CA, (408) 734-8200) is offering the first members of a CMOS product line that operates with a 3.3V supply instead of 5V. The two devices are the P3C3147 4k × 1 and P3C3148 1k × 4 static RAMs, both of which feature 6-nsec read and write cycles. They cost approximately $16 (1000). All the products planned for this family will operate at the reduced voltage. Some advantages of the lower supply voltage, according to the company, include drive compatibility with GaAs circuits and reduced ground bounce. The company expects to introduce additional members of the family during 1989. The additional products will include octal drivers, gate arrays, and the R3000 and R3100 RISC processor and floating-point accelerator.—Richard A Quinnell

XILINX ADDS WORKSTATION SUPPORT FOR XACT

To supplement its support of the XACT development system for Logic Cell Arrays on personal computers, Xilinx (San Jose, CA, (408) 559-7778) is now providing its software on standard workstations from Sun Microsystems (Mountain View, CA, (415) 960-1300), Apollo Computers, (Chelmsford, MA, (508) 256-6600) and DEC (Maynard, MA, (508) 493-5111). The XACT system provides logic synthesis, automatic placement and routing, and schematic capture for design implementations on Xilinx devices.—Michael C Markowitz

ASIC FAMILY ADDS BICMOS AND ECL GATE ARRAYS

The ASIC Div of NEC Electronics (Mountain View, CA, (415) 960-6000) is adding two gate-array families—one bipolar/CMOS (BiCMOS) and one ECL family—to its product offerings. The 67000 BiCMOS array family operates with signal frequencies as great as 200 MHz. The arrays come in 2000-, 3000-, 5000-, 10,000-, and 24,000-gate versions in a variety of package styles. They range in price from $11.50 to $260 (10,000), and samples are available now.

Samples of the uPB63000 family of ECL gate arrays will be available in May. This family features a minimum toggle frequency of 1.4 GHz and can operate at 10KH ECL, 100K ECL, and TTL logic levels. The family members include 2400-, 13,902-, 21,228-, 28,000-, and 35,400-gate versions and range in price from $220 to $833 (1000).—Richard A Quinnell

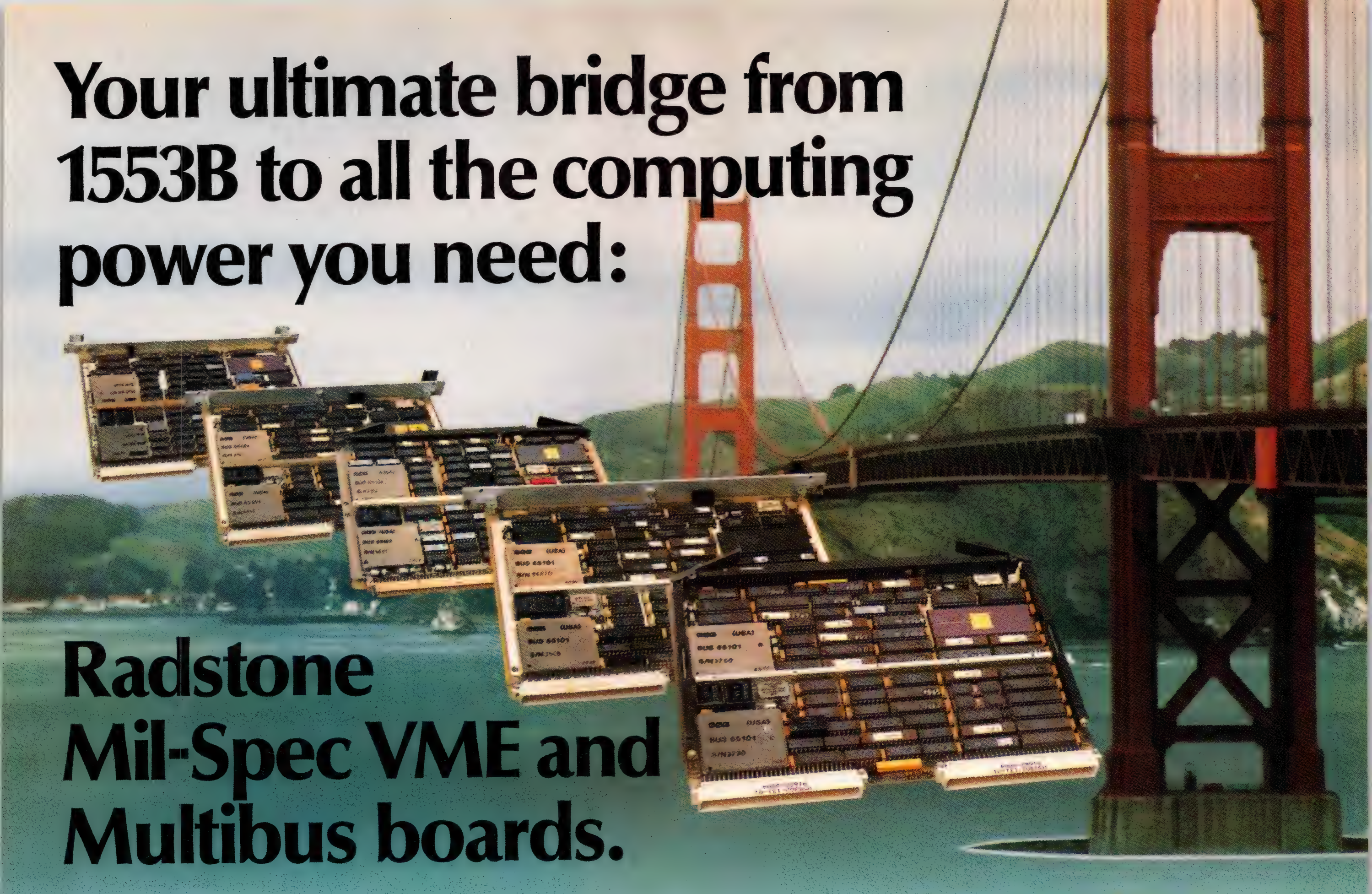
MINIATURE CIRCULAR DIN PLUGS FIT PC KEYBOARDS

For engineers who've had trouble finding miniature circular DIN plugs that are compatible with the IBM PS/2 and Apple Macintosh personal-computer keyboards, Cinch Connector Div (Elk Grove Village, IL, (312) 981-6000) offers a solution. The company now manufactures a line of the diminutive plug components, including insulators, shielded cases, and crimp contacts. It also offers the application tooling required to assemble the plugs. A kit of parts for an 8-position plug costs $0.77 in OEM quantities.—Steven H Leibson

ICs SIMPLIFY COLOR IMAGE PROCESSING

Data Translation (Marlboro, MA, (508) 481-3700) offers a pair of ICs that may simplify color image processing. The DT7910 and DT7911 convert digitized color images from standard RGB (red-green-blue) color coding to HSI (hue-saturation-intensity) color coding, and vice versa, at 15M pixels/sec. The manufacturer claims that HSI coding of color images allows image-processing algorithms to work with single variables. The chips convert 24-bit RGB (8 bits for each color) images to 30-bit HSI images, and vice versa, by using proprietary floating-point division algorithms and external look-up tables. The ICs draw 140 mA at 5V and come in 68-pin PLCC packages at a cost of $63 (1000).—Richard A Quinnell

Your ultimate bridge from 1553B to all the computing power you need:



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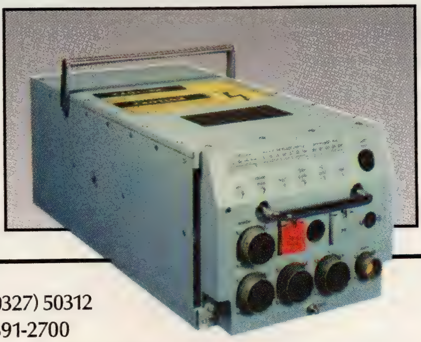

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RADSTONE
TECHNOLOGY

CIRCLE NO 22

NEWS BREAKS: INTERNATIONAL

VME BUS DSP CARD INCLUDES A/D AND D/A CONVERTERS

The VME56000 VME Bus board from Loughborough Sound Images Ltd (Loughborough, UK, TLX 341409) provides a complete digital-signal-processing system, including A/D and D/A conversion, on one double-Eurocard board. The board uses a Motorola DSP56001 DSP chip running at 20 MHz and having 8k words of program RAM and 16k words of data RAM. You can expand the program and data RAMs to 64k words each on the board, and you can configure the data RAM so that as much as 32k words appears in each of the processor's X-data and Y-data memory maps. The board also has two DSP56200 filter chips that you can configure as FIR or adaptive filters.

The 2-channel, 16-bit A/D and D/A converters sample synchronously at 200k samples/sec and come with programmable antialiasing and reconstruction filters, respectively. The A/D converter's inputs also have sample-and-hold circuits. The board operates as either a VME Bus master or a slave, and it has interrupt-handler, interrupt-generator, and system-controller functions. Its development support includes an onboard debug monitor that you can control via a terminal, an RS-232C link, and development-system software that runs on an IBM PC. The company can also provide device drivers for controlling the board from VME Bus CPUs that run Unix. The board costs approximately $6000.—Peter Harold

PLUG-IN UNIT SHIELDS VXI BUS MODULES FROM EMI AND RFI

Bicc-Vero Electronics Ltd (Eastleigh, UK, TLX 47551; in the US: Hamden, CT, (203) 288-8001) has introduced a plug-in unit that's specifically designed to meet the EMI and RFI shielding requirements of VXI Bus instrumentation. The unit is of clamshell construction; it has two U-shaped pressed-steel sections that sandwich a VXI Bus pc board. A conductive gasket along the edges of the two sections, combined with plated through-holes in the pc board, provides an unbroken electrical connection between the case components, ensuring good RFI shielding. The plug-in unit can also include spring contacts that allow you to ground the unit to the ground plane on the VXI Bus backplane, as well as to adjacent VXI Bus modules. Cooling holes with proven RFI-screening performance are provided in the unit. The plug-in unit is currently available as a 6U-high module that costs between £50 and £60 (100). It will also be available as a 9U unit. The company offers heavy-duty card frames to support the extra weight of VXI Bus modules.—Peter Harold

LASER OPTICAL SENSOR SEES THROUGH SMOKE AND FLAME

According to reports in the Japanese press, Matsushita has created a laser optical sensor that can enable a system such as a robot to detect the distances and shapes of objects, even when they're obscured by smoke and flame. To detect an object, the sensor emits a laser beam and observes the beam's reflection, sending the data to a display. The sensor can distinguish the reflected laser signal from such noise as the infrared rays emitted by flame. The device is portable and has an effective range of 30m. It will initially be applied in robots used for rescue and disaster prevention. The firm also plans to offer the sensor for use in buildings and underground tunnels. Eventually, the company expects to develop a smaller, higher-performance version of the sensor for use in factory-automation systems and all-weather navigation systems for automobiles.—Joanne De Oliveira

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INSTRUMENTS OF DISCOVERY

CIRCLE NO 23

SURFACE MOUNT MIXERS

$3.30 (1,000 qty)

The opportunity for automated, low-cost assembly is a key benefit of surface-mount technology, but is often wiped out by the high price of surface-mount components. Now, Mini-Circuits offers a new series of mixers to meet the pricing demands of SMT…only $3.30 in 1,000 quantity ($3.95 ea. in quantity of 10)…at a cost even lower than most conventionally-packaged mixers.

The SCM-1 spans 1 to 500MHz and the SCM-2 covers 10 to 1,000MHz. Housed in a rugged, non-hermetic 0.4 by 0.8 by 0.3 in. high (maximum dimensions) plastic/ceramic package. Spacing between connections is 0.2 in. The mixer is offered with leads (SCM-L) or without leads (SCM-NL) to meet a wide range of pc board mounting configurations.

Each SCM is built to meet severe environmental stresses including mechanical shock/vibration as well as temperature shock. The operating and temperature storage range is -55°C to +100°C. Each SCM, designed and built to meet today's demanding reliability requirements, carries Min-Circuits' exclusive 0.1% AQL guarantee of no rejects on every order shipped (up to 1,000 pieces).

When you think SMT for low-cost production, think of Mini-Circuits' low-cost SCM mixers.

SPECIFICATIONS (typical)	SCM-1L SCM-1NL (L=with leads)	SCM-2L SCM-2NL (NL=no leads)
FREQ. RANGE (MHz)		
LO,RF	1-500	10-1000
IF	DC-500	5-500
CONVERSION LOSS (dB)		
Midband	6.3 dB	6.5 dB
Total Range	7.5 dB	8.0 dB
ISOLATION (dB)	(L-R)(L-I)	(L-R)(L-I)
Low-Band	60 45	45 35
Mid-Band	45 40	35 30
High-Band	40 35	25 20
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LOW PASS **Model**	***LP–**	**10.7**	**21.4**	**30**	**50**	**70**	**100**	**150**	**200**	**300**	**450**	**550**	**600**	**750**	**850**	**1000**
Min. Pass Band (MHz) DC to		10.7	22	32	48	60	98	140	190	270	400	520	580	700	780	900
Max, 20dB Stop Frequency (MHz)		19	32	47	70	90	147	210	290	410	580	750	840	1000	1100	1340

Prices (ea.): Qty. (1-9) P $11.45, B $32.95, N $35.95, S $34.95

HIGH PASS **Model**	***HP–**	**50**	**100**	**150**	**200**	**250**	**300**	**400**	**500**	**600**	**700**	**800**	**900**	**1000**
Pass Band (MHz)	start, max.	41	90	133	185	225	290	395	500	600	700	780	910	1000
	end, min.	200	400	600	800	1200	1200	1600	1600	1600	1800	2000	2100	2200
Min. 20dB Stop Frequency (MHz)		26	55	95	116	150	190	290	365	460	520	570	660	720

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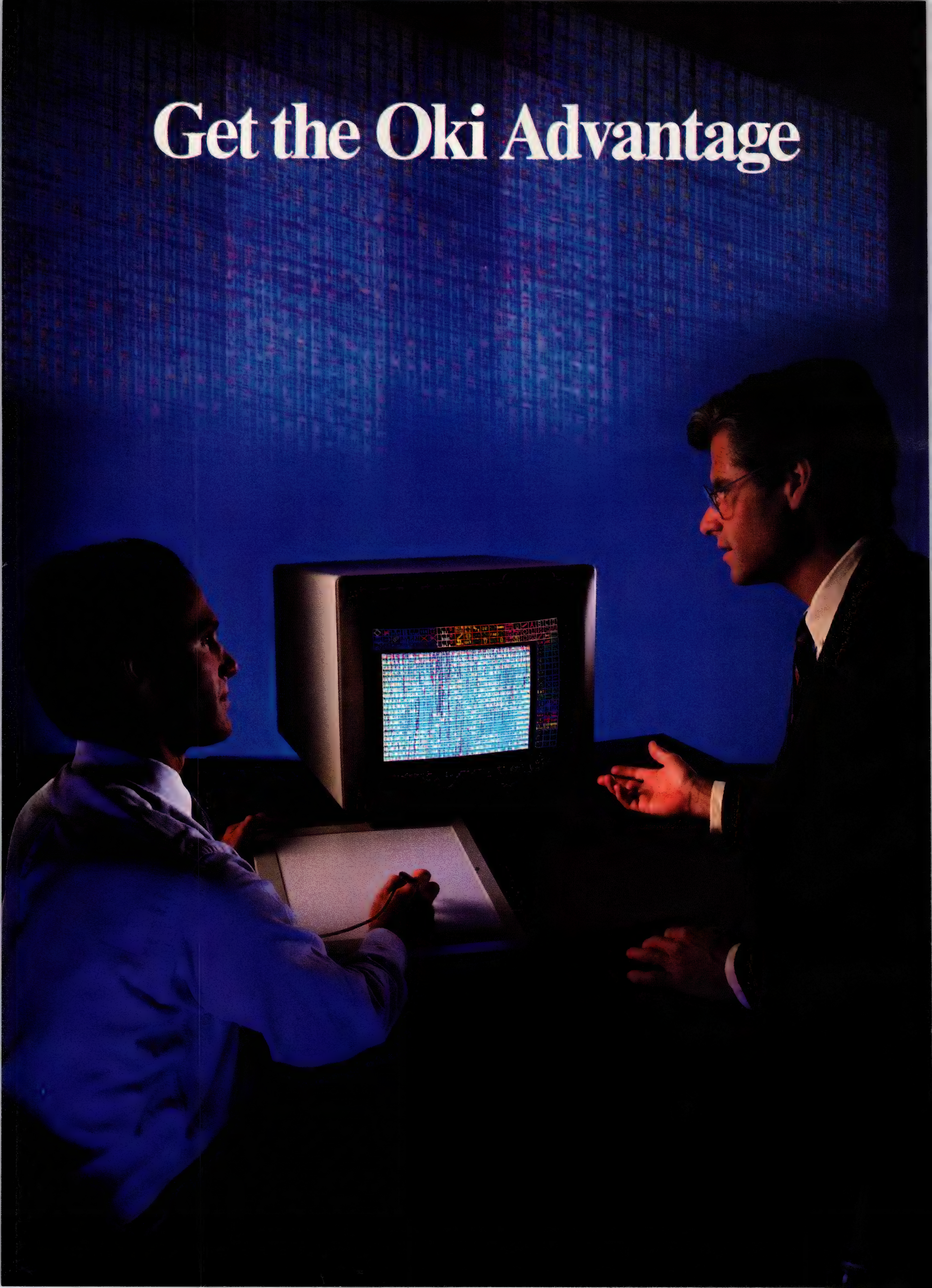
*Prefix P for pins, B for BNC, N for Type N, S for SMA *example:* **PLP-10.7**

C105 REV. E

CIRCLE NO 25



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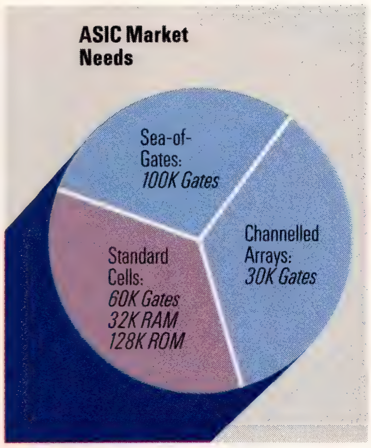

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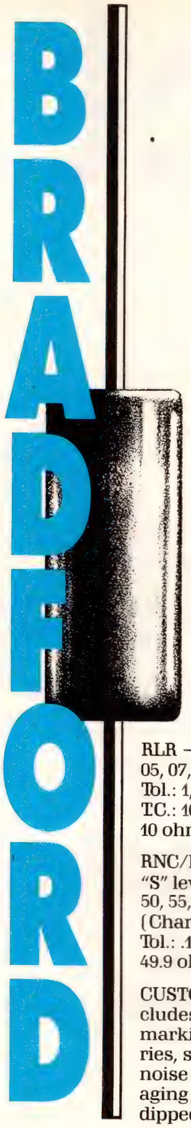

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CIRCLE NO 28

SIGNALS & NOISE

Taking a new perspective

I just finished reading Charles Small's article, "RISCs force move to compilers," (EDN, January 5, pg 73) and would like to pass on my thanks for publishing one of the most clearly written, succinct reports on programming for RISC processors that I have come across.

Too often, I read articles that rely upon seemingly arbitrary product "performance" data supplied by manufacturers (including compiler writers, I might add) to give the impression of depth and completeness in their reports. Charles deserves credit for taking the perspective of the embedded system designer, faced with many confusing choices, who must find a way to successfully integrate these products and solve his problem.

From my vantage point, as one who discusses software development environments with microprocessor companies on an ongoing basis, there are additional issues within this general area that might prove interesting to your readers. Some issues that come to mind include debugging and optimized code, native (Unix or MS-DOS) tools vs cross tools for programming embedded processors, and debugging with on-chip or ROM monitor emulation (especially for RISC chips).

Again, congratulations on a timely and well-written article.

Allen Reedy
Marketing Manager
Development Systems Group
Intermetrics Inc
Cambridge, MA

Errata

Our apologies go out to our readers and to Sergio Franco, whose article, "Current-feedback amplifiers benefit high-speed design," appeared in EDN's January 5 issue (pg 161). Some problems with math symbols in our new typesetting equipment caused errors in his article. Please note the following:

On pg 163, the equation on the line above **Eq 6** should read

$$(1+R_2/R_1)/a_0 \ll 1.$$

The equation on the line above **Eq 14** should read

$$R_2/z_0 \ll 1.$$

On pg 170, the first equation in the right-hand column should be raised to the ½ power, not to the first power.

In several places in the article, a τ appeared where the symbol for resistances in parallel, as in $(R_1 \| R_2)$, should have been. They appear in the right-hand column on pg 166 in the second line of the 4-column formula and three lines above that; in the last line in the left-hand column on pg 167 and the second line following **Eq 16**; in the right-hand column on pg 168 in lines 3, 4, 8, and the last line; and in the left-hand column on pg 170 in lines 1 and 5 and in the line before **Eq 20**.

One human error also occurred: Two lines above **Eq 16** on pg 167, change $V_{OUT}=V_N$ to $V_{OUT}=zI_N$.

YOUR TURN

EDN's Signals and Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

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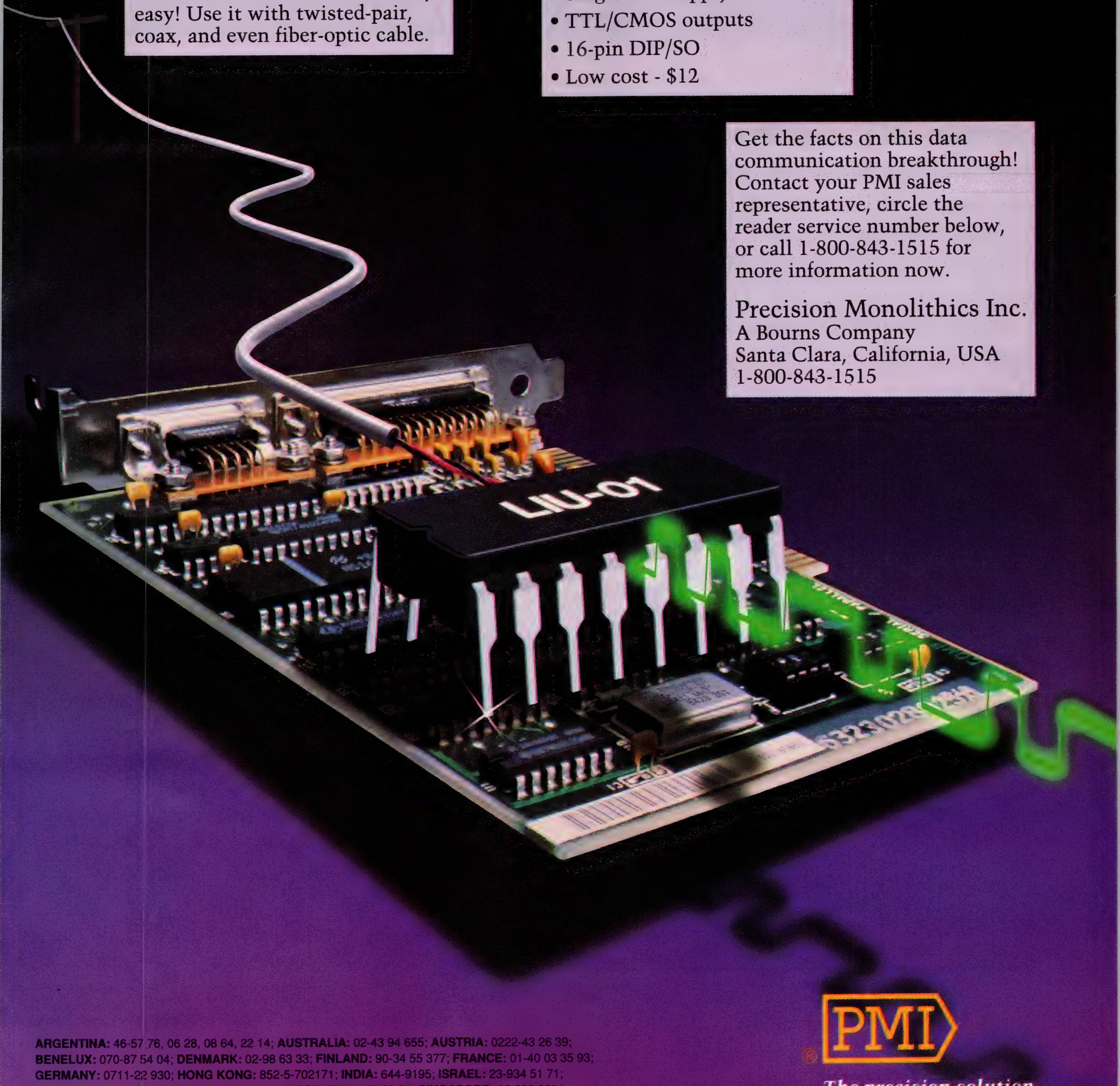

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CIRCLE NO 29

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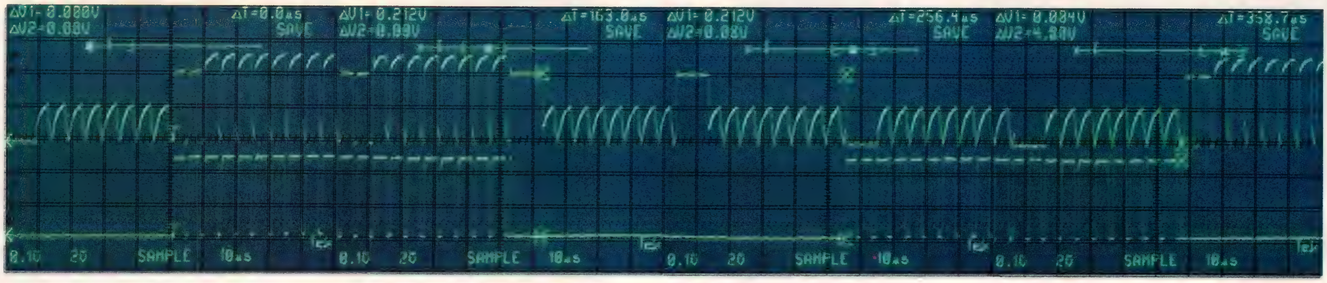

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Record Length	1K/4K Selectable	4K	4K	4K	2K
Glitch Capture	100 ns	100 ns	100 ns	No	No
CRT Readout/ Cursors	Yes	Yes	No	No	No
GPIB/RS-232-C Options	Yes	Yes	Yes	No	RS-232-C Hardcopy
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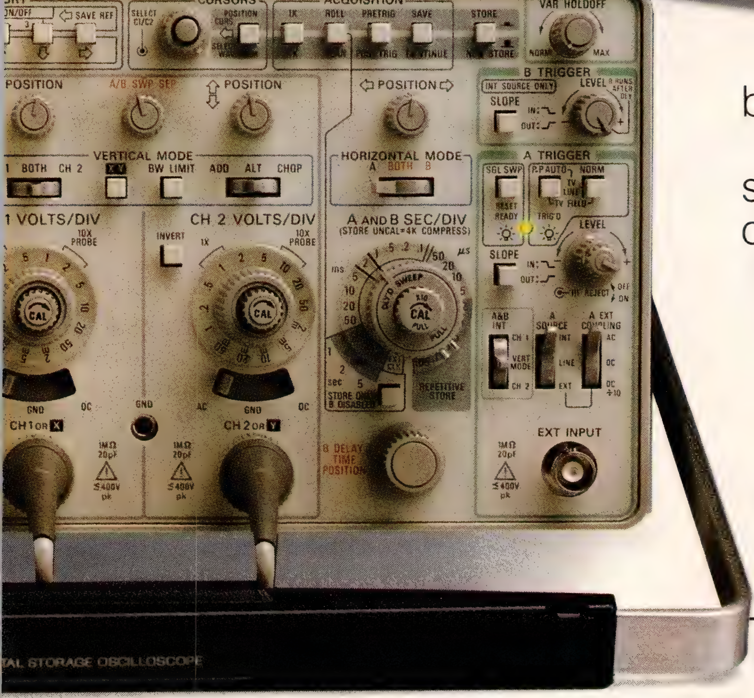
Each scope offers a range of capabilities you'd expect to find only in much more expensive instruments.



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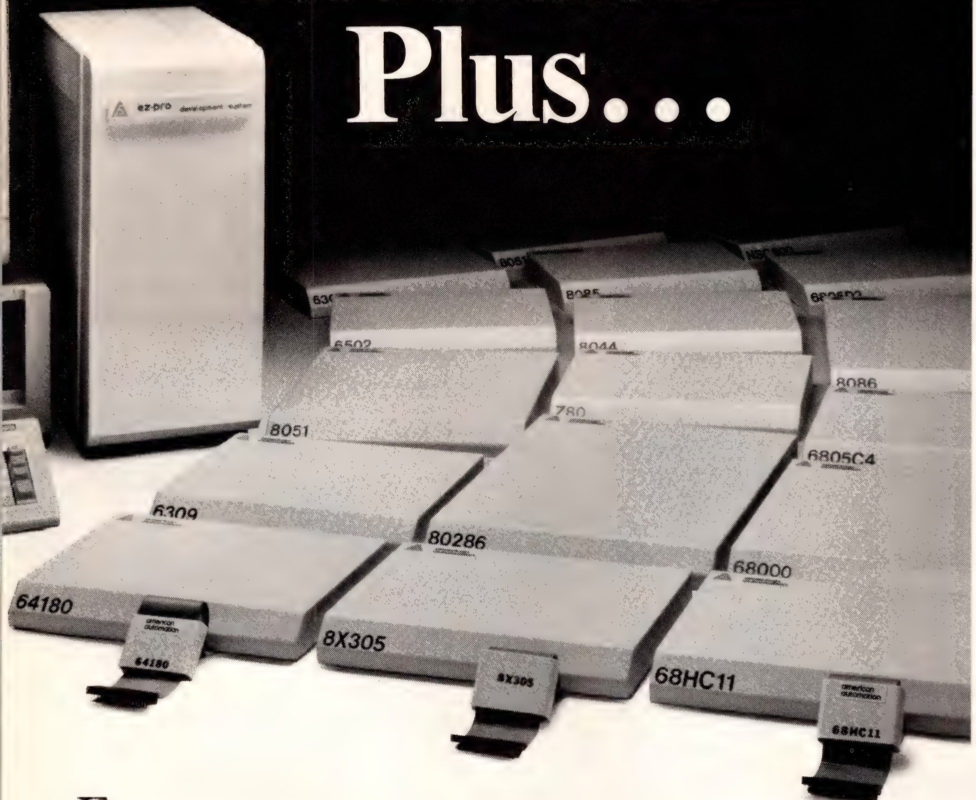

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CIRCLE NO 31

CALENDAR

Commercially Available Reduced-Instruction-Set Computer Processors (seminar), Anaheim, CA. Dr Amnon Aliphas, DSP Associates, 18 Peregrine Rd, Newton, MA 02159. (617) 964-3817. March 1 to 3.

Systems Engineering for Integrated Hardware/Software Applications (short course), Los Angeles, CA. John Valenti, Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (231) 417-8888. March 7 to 10.

The Executive Forum on Supercomputing, San Jose, CA. Pat Westly, Westly Enterprises, 3697 S Court, Palo Alto, CA 94306. (415) 494-7115. March 9 to 10.

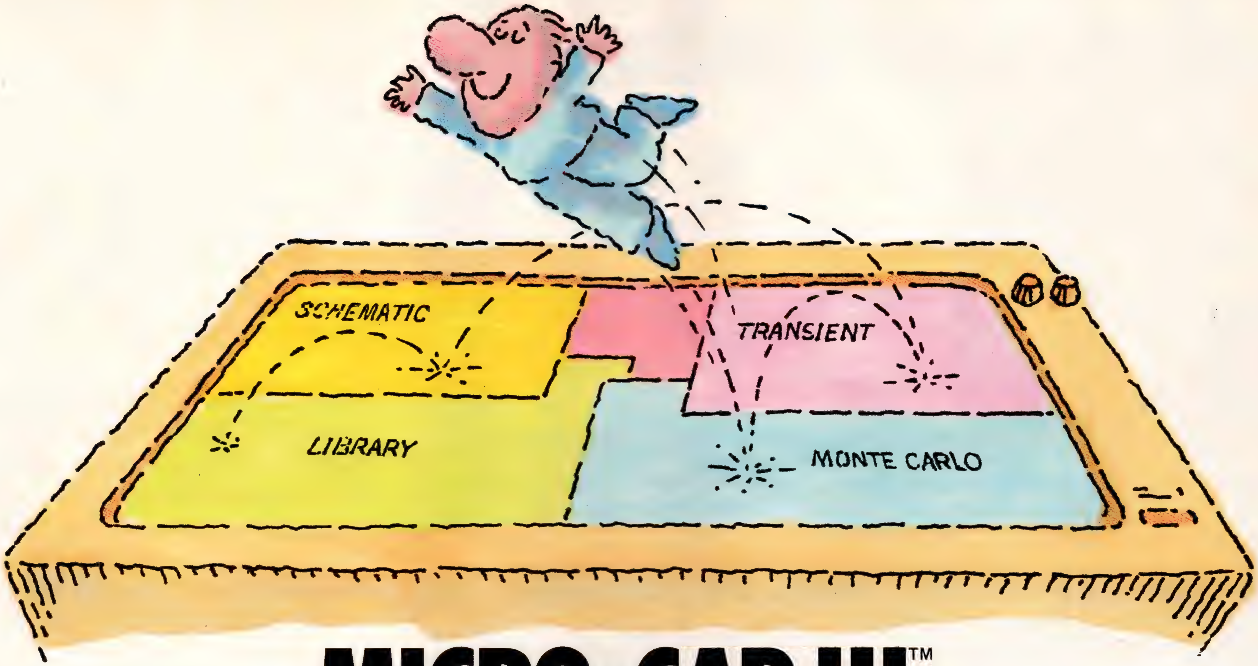
APEC '89 (IEEE Applied Power Electronics Conference and Exposition), Baltimore, MD. Trey Burns, Data General Corp, 4400 Computer Dr, E213, Westboro, MA 01580. (508) 870-9182. March 13 to 17.

C Programming Workshop, Seattle, WA. Specialized Systems Consultants Inc, Box 55549, Seattle, WA 98155. (206) 527-3385. March 13 to 17.

Modern Electronic Packaging (seminar), San Diego, CA. Technology Seminars Inc, Box 487, Lutherville, MD 21093. (301) 269-4102. March 20 to 22.

DCA Forecast to Industry (seminar), Tyson Corner, VA. Janie Herring, AFCEA NOVA Chapter, The BDM Corp, 7915 Jones Branch Dr, McLean, VA 22101. (703) 848-6944. March 27 to 28.

IBM Personal Computer Interfacing for Scientific Instrument Automation (workshop), Blacksburg, VA. Linda Leffel, Donaldson Brown Center for Continuing Education, Virginia Tech, Blacksburg, VA 24061. (703) 961-4848. March 27 to 29.



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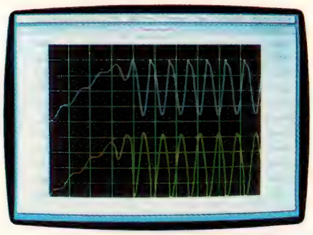
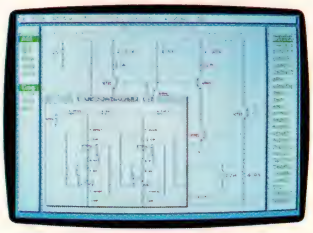


Transient analysis



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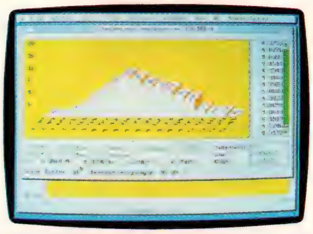

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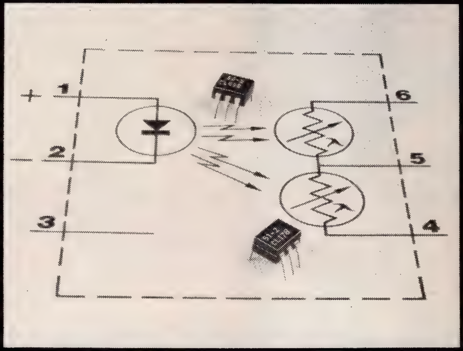

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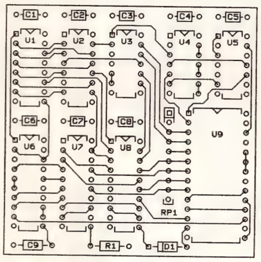

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CIRCLE NO 34

CALENDAR

1989 Technical Symposia on Aerospace Sensing, Orlando, FL. The International Society for Optical Engineering (SPIE), Box 10, Bellingham, WA 98227. (206) 676-3290; in Europe: SPIE, Koblenzer Strasse 34, D-5300 Bonn 2, West Germany. (49228) 361546. TWX 172-283-747. March 27 to 31.

Digital Signal Processing, Single-Chip DSP Processors, Development Systems—Theory, Designs and Applications (seminar), Cambridge, MA. Dr Amnon Aliphas, DSP Associates, 18 Peregrine Rd, Newton, MA 02159. (617) 964-3817. April 3 to 5.

Commercially Available Reduced-Instruction-Set Computer Processors (seminar), Cambridge, MA. Dr Amnon Aliphas, DSP Associates, 18 Peregrine Rd, Newton, MA 02159. (617) 964-3817. April 5 to 7.

Electronic Imaging Conference West, Pasadena, CA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. April 10 to 13.

Modern Electronic Packaging (seminar), Baltimore, MD. Technology Seminars Inc, Box 487, Lutherville, MD 21093. (301) 269-4102. April 18 to 20.

12th Annual IEEE Design for Testability Workshop, Vail, CO. T W Williams, IEEE Subcommittee on DFT, IBM Corp, Box 1900, Boulder, CO 80302. April 18 to 21.

The Computer-Aided Software Engineering Symposium (CASES), Boston, MA. Elizabeth C Barnaby, Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 475-6990. April 24 to 26.

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TURN TO
PAGE 222

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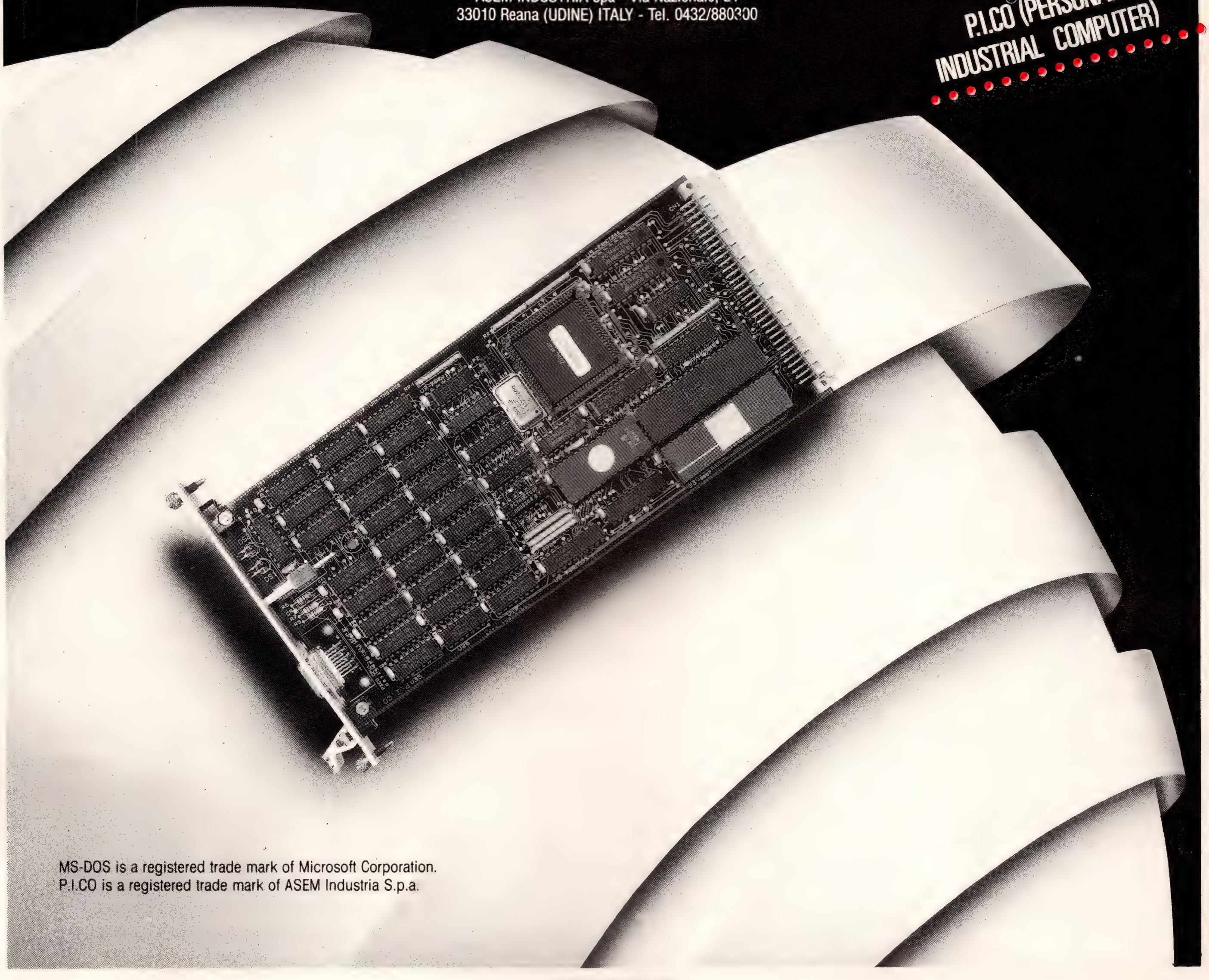

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CIRCLE NO 39

EDITORIAL

Coordinate science and technology R&D

The US National Academy of Sciences recently reported that we have lost effective coordination of our $60 billion science and technology budget. Half of the budget goes into military R&D projects that may have little commercial applicability. But the remaining $30 billion goes into research efforts that could show commercial promise if we knew what research we were doing. Today, we're spending government money duplicating and redoing research while simultaneously missing research opportunities. Thus, we're wasting money, time, and talent. Our science and technology efforts deserve better.

Japan's Ministry of International Trade and Industry (MITI) coordinates many research projects. The US has no equivalent agency to watch over and coordinate federal R&D spending. That is unfortunate. A glance at the list of US government departments reveals that there is great potential for duplicating research efforts. For example, most of the cabinet-level departments—Agriculture, Commerce, Defense, Energy, and Health and Human Services—have their own research programs. These programs fund internal research efforts as well as those taking place in private industries and universities. Today, it's possible for the National Institutes of Health to fund a project similar to one already being sponsored by the National Science Foundation.

It's time for our government to set clear priorities for the research it funds, and a cabinet-level Department of Science and Technology is the place to start. Although I dislike expanding our government by adding another bureau, after looking at the crazy-quilt pattern of research-funding groups, I think that a strong coordinator could make a difference. Here's a partial list of the US government groups that could coordinate their activities and budgets through such an overseer:

- National Institute of Standards and Technology
- National Technical Information Service
- National Telecommunication and Information Administration
- Defense Advanced Research Projects Agency
- National Institutes of Health
- Consumer Products Safety Commission
- Environmental Protection Agency
- National Aeronautics and Space Administration
- National Science Foundation
- Nuclear Regulatory Commission
- Federal Communications Commission

In fact, it might pay to meld all of the various research agencies, bureaus, and commissions into a Department of Science and Technology that would serve the other government agencies. Businesses could benefit, too, by easily determining what publicly funded work was underway and who was doing it. They might find someone working on a project similar to one they'd like to undertake. Likewise, they might find opportunities in areas devoid of development work.

There's one negative side to this proposal. Excellent leaders with a national vision and a sense of mission for science and technology are hard to find.

Jon Titus

Jon Titus
Editor

Jesse H Neal
Editorial Achievement Awards
1987, 1981 (2), 1978 (2),
1977, 1976, 1975

American Society of
Business Press Editors Award
1988, 1983, 1981

Signetics 68070

Moto dives into RISC chip pool

NEW YORK—Motorola finally takes its plunge into the RISC pool today announces its long-awaited chip set. More

chip from a semiconductor manufacturer to find a place in the computer and workstation world. Major system companies are pushing the RISC theme with own architectures, shutting door on standard products

Advanced Micro Devices positions its 29K for the embedded micro mar

AMD, with its new 29000 mi bably the most recep

Intel unveils long-awaite

Intel Corp. of Santa Clara unveiled on Thursday its long-anticipated 'P-9' computer chip, which will create less expensive personal computer systems that run more sophisticated software.

Introduction of the new 80386SX chip, which analysts say eventually will supplant Intel's widely used 80286 chip as the "brain" of certain IBM PC and compatible computers, essentially is a marketing move that allows computer makers to offer lower-cost alternatives in their high-powered 80386-based product line.

For example, prices o puters—like the IBM 80286—range from $4,500. Systems bas like the IBM Mod chip—start at ab The 80386SX all the software of —although more slow The new chip also w 8086 software, Intel said. While analysts said they expe

er 386

the 80286 chip in many they also the huge market machines, larly lower-ish. han 10 million 8028 directly upgrade 386SX chip. But called can

32 micro now supported by fast coprocessor control chip

Although National Semiconductor's NS32532 microprocessor has a dedicated math coprocessor (the NS32381), its 1-MFLOPS floating-point calculation speed is deemed too slow for many tasks. To meet speed demands, National came up with the NS32580,

a dedicated coprocessor-control chip that ties Weitek's WTL3164 fast floating-point data path in the 32-bit 32532 microprocessor. The combination yields a peak floating-point performance of 15 MFLOPS for single- and double-precision tasks.

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CIRCLE NO 40

TIME-MEASUREMENT INSTRUMENTS

A mature industry returns to innovation

New features and ways of measuring arouse a dormant technology.

Dan Strassberg,
Associate Editor

Just as no data-processing manager ever lost his job for buying an IBM mainframe, no test engineer ever lost his job for choosing a counter from Hewlett-Packard.

But the safest solution may not be the only good one, particularly when you're shopping for a counter/timer or a time-interval analyzer. HP dominates the time-measurement market and has earned a reputation for sound design, quality construction, and excellent postsale support. Nonetheless, if you limit yourself to HP products, you can easily miss some of the reasonably priced, well-designed, and well-built instruments that other manufacturers offer.

Time measurement is a mature market: Digital counters and counter/timers have been around for decades, and over the years engineers have developed dozens, perhaps hundreds, of variations on basic time-measurement schemes. But don't assume that all recent developments in time-measurement technology are only incremental improvements; some products actually break new ground.

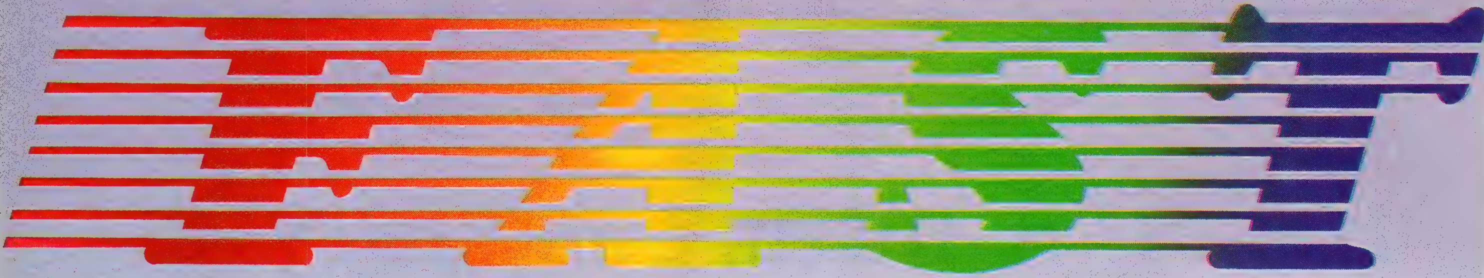
Interval duration vs time

Last year, when HP brought out its 5371A frequency and time-interval analyzer, it introduced the idea of the modulation domain, which lets you record and display variations in time intervals, phase, and frequency, as a function of time. With some justification, the company announced when it introduced the 5371A that it was "about time" that you could make such measurements. In fact, time-interval analysis is probably the most important recent extension of time-measurement technology.

However, the 5371A was not the first interval analyzer, although it was the first and is still the only instrument to make certain types of measurments.

Not only can it display frequency and time measurements, *HP's 5371A displays how successive measurements vary over time. It also makes many calculations on the acquired data.*

Run ECL



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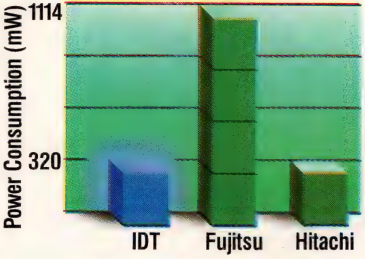

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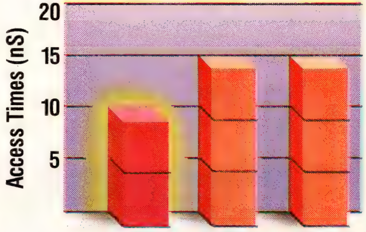
Speed Comparison



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CIRCLE NO 41

Time-measurement instruments

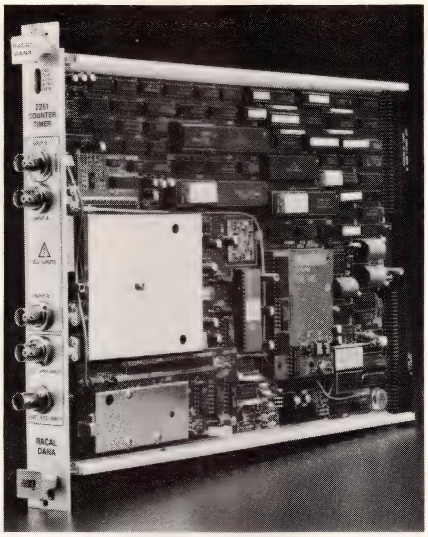
The 2001A and 3100 time-interval analyzers from Kode and the SR620 universal counter/timer from Stanford Research Systems, among others, can construct and let you display histograms of time-interval durations (see **Table 1**). The 5371A, however, can display how the length of the intervals varies with time to determine such issues as whether the variations are random or periodic, and whether the intervals decrease or increase monitonically.

Look ma, no gaps

Furthermore, the 5371A makes measurements that are continuous, which guarantees that it won't, for example, accidentally miss a fleeting phase change in a frequency-agile communications link. Some other counters contain D/A converters that drive strip-chart recorders and thus let you display the trend in a series of interval measurements, but only the 5371A displays the trend of a series of measurements made with no dead time between them.

Keeping track of the value of every measurement in a long series, as the 5371A does, demands large amounts of memory—particularly when the measurements have the number of digits of precision that time measurements often do. (The 5371A can store 1000 measurements.) Therefore, if you only need histograms, then you may not need the 5371A. A less expensive instrument that just accumulates statistical information and that can provide data on much larger groups of equally spaced measurements might probably do the job for you.

Kode's time-interval analyzers, for instance, construct histograms, determine which "bucket" (range of values) each measured value belongs in, and keep track of the number of measurements in each bucket. The number of buckets is nearly always much smaller than the number of measurements. What's more, the number of digits used to count the measurements in a bucket is usually much smaller than the number of digits in a measured value. Thus, storing histogram data demands much less memory than storing actual measurements does.

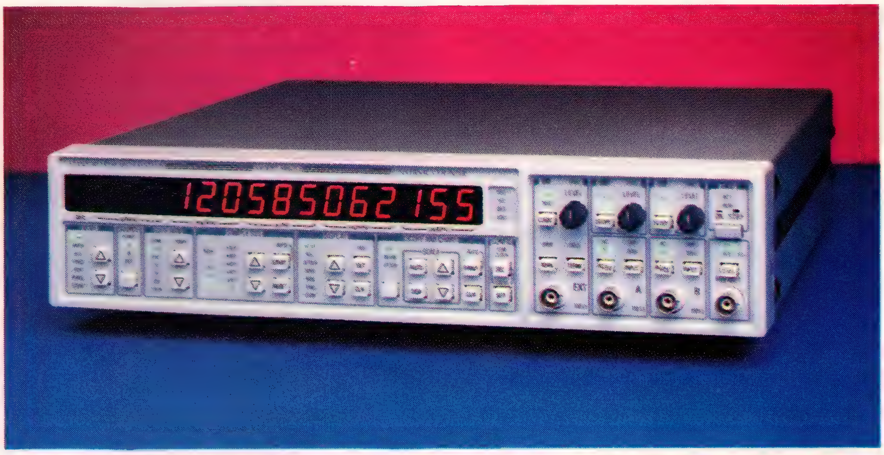

The VXI Bus may change the way instruments look. *The first VXI Bus counter timer is Racal-Dana's 2251.*

Even though the HP 5371A is rather expensive and has been available for only about a year, it has already left an indelible imprint on the field of time measurement: Its capabilities were badly needed, so despite its $21,500 price ($34,500 if you add the 5364A prescaler that extends the instrument's frequency range to 18 GHz), test engineers have greeted it enthusiastically. And HP's use of interval analysis in its own product has opened up a new area for smaller companies too. Companies that before had only been able to sell the concept in specialized areas can now approach a broader market. The result should be a spate of interval analyzers with a whole spectrum of capabilities.

Not only will there be more interval analyzers, but if software from Data Physics Corp is any indicator of future trends, there will also be a number of third-party software packages to manipulate the data gathered by the new instruments. Data Physics' DP280 package runs on HP 9000 Series 200 and 300 computers and performs phase-noise and jitter analysis on data acquired by the 5371A. The software sells for $3000.

Value is improving with time

In addition to offering new kinds of products, the time-measurement area is also moderating the cost of some standard features. Some new products offer specifications previously available only in higher-priced



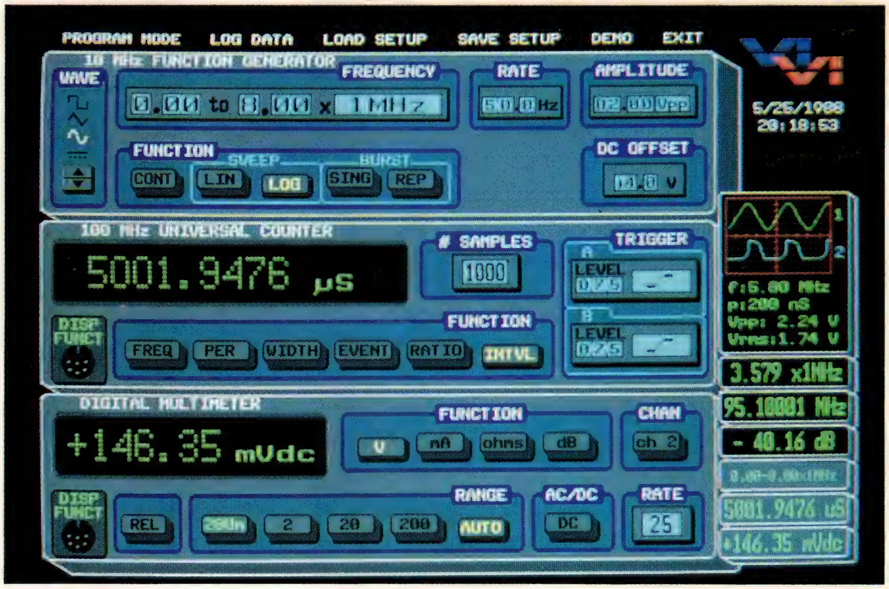
Sporting a 16-digit display, *Stanford Research's SR620 has 25 psec rms single-shot measurement uncertainty and includes firmware-based autocalibration.*

products. Others have added new features, especially autocalibration (similar to the popular feature in top-of-the-line DMMs) and computational powers. Moreover, a substantial number of counter/timers now incorporate a DVM function, which is particularly useful for measuring trigger levels.

Taking one step beyond the inclusion of DVMs, the scope leader Tektronix now offers counters in scopes. The 11301A ($8550) includes a 750-MHz counter in an analog scope with a 400-MHz bandwidth; the 11302A ($12,950) is similar except that the scope offers a 500-MHz bandwidth and incorporates Tek's Microchannel Plate CRT for an extremely high writing rate (6 cm/nsec). Along with the waveforms, both models display the counter's 10-digit output on their screens. Because you usually use a scope and a counter together, the combination is extremely useful.

Combining a counter and a scope is just one of the packaging innovations affecting counter/timers. Other packaging ideas, such as the VXI Bus (VME extentions for instrumentation bus), are bidding to displace conventional rack-and-stack instruments in systems. Moreover, it's no surprise that some time-measurement instrument vendors are favoring PC-based instruments that use a computer's graphics display to simulate an instrument's front panel. To date, however, most of the large number of PC-based counter/timers are low-end products. Few PC-based counter/timers match the specifications of even those instruments that qualify as basic universal counters. One exception is the counter that forms a part of the 325 module from Virtual Instruments (see **Table 1**).

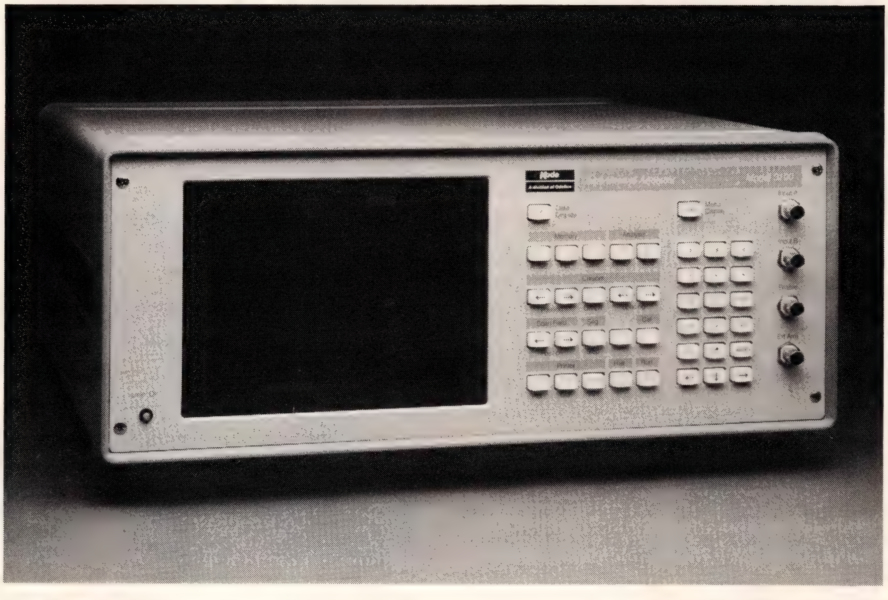
For repetitive-signal measurements, many counters include prescalers (frequency dividers) either as a standard feature or as an option.



Using a PC-based counter/timer, *for example Virtual Instruments' 325, you can display what looks like a standard instrument panel on your PC's monitor. The 325 includes a DMM and a waveform generator, too.*

Prescalers can extend the range of frequencies a counter measures into the GHz region. Even some relatively inexpensive counters now have this feature; their vendors see a great opportunity in the servicing of cellular-telephone equipment.

As in many mature markets, the counter/timer market is highly segmented. HP's 1989 catalog divides the company's offerings into seven categories: basic frequency counters, microwave and millimeter continuous-wave counters, microwave and millimeter pulse counters, basic universal counters, high-performance universal counters, precision time-interval counters, and the frequency and time-interval analyzer. Vendor classifications vary, but the



This time-interval analyzer, *Kode's 3100, generates histograms on groups of measurements.*

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instruments in **Table 1** fall into one of the last five of these categories—or they are bus-oriented modules. Products in another category, panel-mounted system components, are useful in industrial-control applications, but most of those components lack the performance level and features of basic universal counter/timers.

The market's segmentation may or may not help you in choosing an instrument that fits your application. If you don't know exactly what you might need, and if your budget permits, you can, of course, go right to the precision time-interval counter category. If, on the other hand, you know you can only spend a limited amount, you can see if one of the basic universal counters is adequate.

If you're unfamiliar with counter/timers altogether, one of the first areas that's quite likely to confuse you is what constitutes a time-interval measurement instrument. Clearly, if it is to measure time, a counter must be able to provide an output in units of seconds and frac-

TABLE 1—REPRESENTATIVE TIME-MEASURING INSTRUMENTS

VENDOR	MODEL	DIGITS	1-SHOT INTERVAL RESOLUTION (nSEC RMS)	MAX FREQUENCY (Hz)	SENSITIVITY (mV)	TIMEBASE		BASE PRICE	COMMENTS
						AGING RATE PPM/TIME	THERMAL (PPM 0-50°C)		
BECKMAN INDUSTRIAL	UC10	8	100	100M	20	1/MONTH	±20	$339	
COLORADO DATA SYSTEMS	53A-541	8½	100	10M	100	0.1/MONTH	4	$1495	INSTRUMENT ON A CARD. FITS VENDOR'S CHASSIS.
FLUKE									SEE PHILIPS. FLUKE SELLS PHILIPS PRODUCTS IN THE U.S.
HEWLETT-PACKARD	5315A	8	100	1G	10	0.1/MONTH OPTIONAL	±1 0-40°C OPTIONAL	$1250	CATALOG LISTS 26 TIME-MEASURING INSTRUMENTS. 15 MEASURE INTERVALS.
	5335A	12	2	1.3G	35	0.0005/DAY OPTIONAL	0.007 OPTIONAL	$4400	INCLUDES DVM.
	5370B	16	20 pSEC	100M	35	0.0005	0.007	$11,000	
	5371A	10	150 pSEC	500M; 18G OPTIONAL	15	0.2/YEAR	NOT SPECIFIED	$21,500	FREQUENCY AND TIME-INTERVAL ANALYZER. SEE TEXT.
KODE	TIA 2001A	4.8	1 nSEC FASTEST TIMEBASE			NOT SPECIFIED		$15,000	TIME-INTERVAL ANALYZER FOR DISK DRIVE TESTING
	3100	1 PART IN 4000	100 pSEC FASTEST TIMEBASE			0.001% ACCURACY 50 pSEC JITTER		$22,500	TIME-INTERVAL ANALYZER. SEE TEXT.
PHILIPS	PM6652C PM6654C	9½ SAME	100 2	BOTH: 120M WITH 1.5G OPTIONAL	60 P-P	0.01/ MONTH OPTIONAL	0.005 OPTIONAL	$2280 $2500	UNITS SIMILAR EXCEPT FOR CLOCK. PM6652C: 10 MHz; PM6654C: 500 MHz. UNITS CAN DISPLAY TRIGGER LEVEL. CATALOG LISTS 23 COUNTERS. 11 MEASURE INTERVALS. FLUKE SELLS PHILIPS PRODUCTS IN THE U.S.
RACAL-DANA	2251	9	1	160 MHz 1.3 GHz OPTIONAL	25 RMS	USES VXI-BUS 10-MHz CLOCK. STAND-ALONE UNITS CAN HAVE OPTIONAL TIMEBASES WITH 0.0005 PPM/DAY AGING AND 0.007 PPM STABILITY FROM 0 TO 50°C.		$3250	C-SIZE VXI-BUS MODULE. VENDOR MAKES A BROAD LINE OF COUNTER/TIMERS IN CONVENTIONAL PACKAGES AS WELL AS CARD-LEVEL UNITS IN OTHER FORMATS.
SIBEX	FC-1	8	1000	10M	←NOT SPECIFIED→			$92.95	HANDHELD, BATTERY-POWERED UNIT
STANFORD RESEARCH	SR620	16	25 pSEC	1.3G PRE-SCALERS STANDARD	35 RMS	0.0005/DAY OPTION	0.005	$3850	INCLUDES DVM TO MEASURE TRIGGER LEVELS. DIRECT INPUTS TO 200 MHz.
TEKTRONIX	DC 510	9	3.125	350M	25 RMS	4/YEAR	±0.2	$3300	MODULAR INSTRUMENT. PLUGS INTO TM 500 MAINFRAME. HAS DVM TO MEASURE TRIGGER LEVELS.
	DC 5009	8	10	135M	20 RMS	1/YEAR	±0.2	$1900	MODULAR INSTRUMENT. PLUGS INTO TM 5000 MAINFRAME. BESIDES UNITS SHOWN, VENDOR OFFERS FIVE MODELS.
	11301A 11302A	10	2	750M	100 P-P	1/YEAR	±0.2	$8550 $12,950	COUNTER IN 400-MHz SCOPE. RESULTS SHOWN ON SCREEN. SAME EXCEPT 500-MHz SCOPE HAS HIGHER WRITING RATE.
VIRTUAL INSTRUMENTS	325	8	0.1 (AVERAGE OF 1k MEASUREMENTS)	10M; 100M WITH PRESCALER	75 RMS	NOT SPECIFIED; ACCURACY ±1.5 PPM		$2995	PLUG-IN CARD FOR IBM PC BUS. ALSO INCLUDES SINE/SQUARE/TRIANGLE-WAVE GENERATOR AND 4½-DIGIT DMM.

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	AMC	Intel
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▶ VALIDATE/Soft-Scope is a complete in-circuit source level debugger that shows variables, data structures and assembly instructions	✓	
▶ VALIDATE/Soft-Scope has in-circuit source level debug capability in 286 protect mode	✓	
▶ Tool chain supports Microsoft C (Also other versions of C and Pascal, FORTRAN, PL/M, Assembler, Jovial)	✓	
▶ Add processor support by merely adding emulator board and probe module	✓	
▶ Has unlimited breakpoint capability	✓	
▶ Over a megabyte of overlay memory is available	✓	

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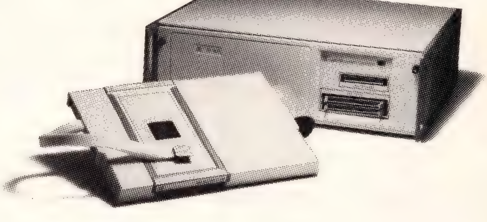

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CIRCLE NO 43

tions thereof—and not just in multiples of a Hz. However, by industry convention, expressing results in units of time, though necessary, is not enough; an instrument must also have separate start and stop inputs. A counter that reads out in time but that has just one input is said to measure "periods" as opposed to "time intervals."

Analyze your needs carefully

What constitutes a time interval is just the beginning of the confusion. Knowing the particular requirements of your application is perhaps more important when choosing a counter/timer wisely than it is when choosing other instruments. Furthermore, you have to be able to interpret the standard specifications, both in a general sense and for individual devices. You should be aware of how the industry's specification conventions can cloud and stretch the truth (sometimes, in fact, they're downright ambiguous). And you need to know in detail how those products that especially interest you actually perform.

Throughout the electronics industry, a perverse law seems to reign: The meaningless specifications drive the meaningful ones out of currency. To be fair, the vendors of high-performance counters, like HP and Stanford Research, are sensitive to the confusion that counter/timer specifications can cause. In an effort to relieve that confusion, they now refer to the specification that used to be named "resolution" as "the least-significant digit," and they often refer to the "single-shot time-interval resolution" instead of "rms jitter."

An excellent example of how difficult it is to interpret counter/timer specifications is the process you must go through to determine a counter's single-shot time-interval resolution. This figure tells you the smallest meaningful difference among individual measurements of presumably equal intervals; because the intervals don't occur often enough, you can't take advantage of the noise reduction you could otherwise obtain from averaging multiple measurements.

One of a number of counters *that incorporate DVMs to measure trigger levels is the PM 6654C from Fluke in the US and Philips in Europe.*

To determine the resolution and accuracy of the measurements made with high-performance counters, not only must you understand the real meaning of the items in the counter's specifications, but you must also make a series of calculations. For example, from your signal's slew rate, you might have to calculate the trigger uncertainty. Then you would use the trigger uncertainty to calculate the resolution.

When you're determining the length of a one-shot event, you must remember that the random noise sources within a counter affect the measured value. So even though the counter's least-significant digit may suggest that it can make a single measurement with 4-psec resolution, the random noise or jitter superimposed on this measurement (that is, the measurement uncertainty) may equal 25 psec rms. When making a small number of measurements, it's not the rms uncertainty that's important; it's the peak-to-peak uncertainty. So, you need to apply a factor to convert from rms to peak-to-peak. A commonly used factor is 6, which represents the 3-sigma points of a Gaussian distribution (the points within which 99.7% of all readings fall). Applying this factor leads to an uncertainty of 150 psec, which is still a really good figure, but a far cry from the 4 psec you started with.

The noise sources in the counter are probably truly random (or very close to random), so if you average a number of measurements (n) you can reduce the uncertainty in proportion to $\sqrt{n}$. If you have enough time when measuring the duration of a repetitive signal, you can let the counter average many measurements. By averaging, counters can legitimately obtain truly impressive

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CIRCLE NO 44

resolution. For example, by making two 1-sec sequences of measurements on an interval or period of 10-µsec duration, the best counters can resolve a 1-psec difference in the measured value, which is the equivalent of less than 100 parts per billion (ppb).

An area of counter specs that may be less confusing but is no less important involves an instrument's timebase. No counter is any better than its timebase. Even if you don't need absolutely accurate measurements, should you need to compare measurements made at different times, or make very accurate measurements that take several seconds, you must be concerned with the timebase's aging rate, short-term stability, and temperature stability.

Inexpensive universal counters *can still have lots of capability, as Beckman Industrial's UC10 demonstrates.*

The quartz crystals that form the heart of a counter's timebase are actually mechanical resonators. Their resonant frequencies drift over time (albeit not very much). For example, the oven-stabilized reference that you can obtain as an option in Stanford Research's $3850 SR620 counter/timer, ages per day at the rate of 0.5 ppb/day. But the drift in one sec, sometimes called the Allan variance, is 0.05 ppb. That means the Allan variance is smaller than the aging rate by a factor of 10—not by the much larger factor of 86,400 you might expect, given that a day contains 86,400 secs. For measurements that stretch over several seconds, such as when you're averaging many readings, a reference's Allan variance can be a significant part of the measurement uncertainty.

In one year, a reference might drift by as much as 365 times the 1-day aging spec, but usually it drifts less. In any event, you can determine how often you need to calibrate your counter by dividing your measurements' absolute-accu-

For more information . . .

For more information on the time-measurement instruments discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

Beckman Industrial Corp
3883 Ruffin Rd
San Diego, CA 92123
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TLX 249031
Circle No 708

Colorado Data Systems Inc
3301 W Hampden Ave, Unit C
Englewood, CO 80110
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TWX 910-933-0193
Circle No 709

Data Physics Corp
1210 S Bascom Ave, Suite 224
San Jose, CA 95128
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FAX 408-977-0801
Circle No 710

Hewlett-Packard Co
19310 Pruneridge Ave
Cupertino, CA 95014
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Circle No 711

John Fluke Mfg Co Inc
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(800) 443-5853, ext 77;
in WA, (206) 347-6100
TLX 185102
Circle No 712

Kode Div of Odetics Inc
1915 S Manchester Ave
Anaheim, CA 92802
(714) 758-0400
Circle No 713

Philips Test and Measurement
Bldg HKF
5600 MD
Eindhoven, The Netherlands
Phone local office
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Racal-Dana Instruments Inc
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Irvine, CA 92718
(800) 722-3262
FAX 714-859-2505
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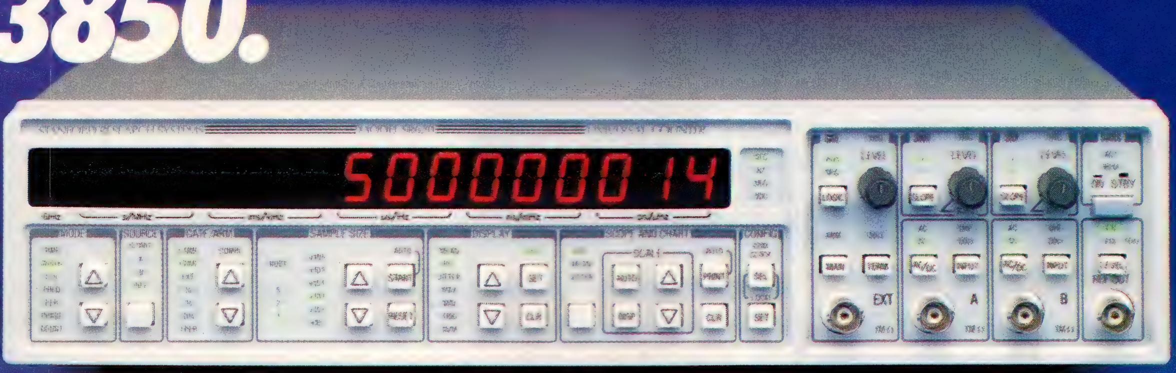
Sibex Inc
1040 Harbor Lake Dr
Safety Harbor, FL 34695
(813) 726-4343
FAX 813-726-4434
Circle No 716

Stanford Research Systems Inc
1290D Reamwood Ave
Sunnyvale, CA 94089
(408) 744-9040
TLX 706891
Circle No 717

Tektronix Inc
Box 1700
Beaverton, OR 97077
(800) 835-9433, ext 170
Circle No 718

Virtual Instruments Corp
23 FJ Clarke Cir #5
Bethel, CT 06801
(203) 748-2000
TLX 493 0512
Circle No 719

Time interval measurement. $3850.



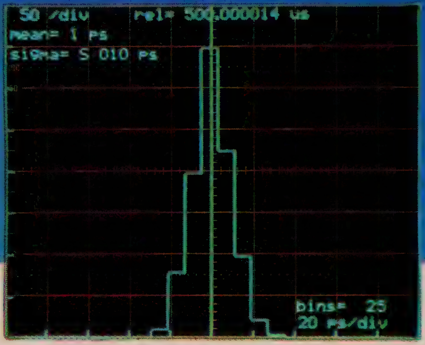
4 ps single-shot resolution
1.3 GHz frequency response
Statistics, analysis, and graphics

Finally, high resolution time interval measurement at an affordable price. The SR620 Universal Time Interval Counter offers 4 ps single-shot LSD on time intervals, and 11 digits of frequency resolution in one second. With powerful arming, gating, and triggering modes, the SR620 can measure time interval, frequency, period, pulse width, and phase, as well as rise and fall times.

The SR620 has built-in statistical functions, including mean, min, max, standard deviation, and Allan variance for up to 1 million samples. Results may be displayed on the front panel, and graphed in histogram or strip chart form on an X-Y oscilloscope. Hardcopy is directly available on a plotter, printer, or chart recorder.

With both RS-232 and GPIB interfaces standard, the SR620 is also ideal for ATE applications.

Whatever your time or frequency measurement needs may be, the SR620 is the answer. For more information, call us at **(408) 744-9040.**



The SR620 provides graphic display of histograms and strip charts on any X-Y oscilloscope. With Autoscale and Zoom, graphics can be easily scaled. Attach a dot matrix printer or an HP-GL plotter and obtain hardcopy of any graph.

SR620	**$3850**
Single-shot resolution	4 ps
Time interval jitter	20 ps rms
Maximum time interval	1000 s
Maximum frequency	1.3 GHz
Frequency resolution	10^{-9} Hz
Phase resolution	0.001°
Statistics	Mean, Min, Max, Std. Dev, and Allan Var.
Sample size	1 to 10^6
Analyzer	Display on X-Y scope
Graphics	Histogram and Strip Chart
Hardcopy	Printer/Plotter
Interfaces	GPIB and RS-232
Oven Timebase (5×10^{-10}/day)	**$950**

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racy requirement by the reference's aging rate. To make sure that a counter's reference oscillator actually performs within its aging spec, you should use the counter only after the oscillator has had the opportunity to stabilize thermally; some vendors tell you to allow 24 or even 48 hours after the application of power for thermal stabilization. In most high-quality counters, the oscillator continues to receive power as long as the counter is connected to the ac line—even if the instrument's main power switch is off. If possible, you should leave such counters connected to the ac line all the time.

Don't assume that because a counter's reference crystal is enclosed in a proportional oven, the instrument's accuracy is totally immune to temperature variations. Over an ambient temperature range of 0 to 50°C, an oven-stabilized oscillator's frequency can change by 10 or more times the figure specified for 1-day aging. Over the same temperature range, a crystal that operates at room temperature can drift by an amount that is hundreds of times its 1-day aging figure. And usually, the aging specification of a room-temperature crystal is inferior to that of an oven-stabilized crystal.

There are very few areas of electronics where new developments no longer occur. Just because a technology or a market mature, don't assume that it's static. As electronic specialties go, time measurement has reached a venerable age, but it continues to change and grow. If you keep an eye on the vendors who serve the market and their product offerings, you may be surprised at the significant advances you'll see.

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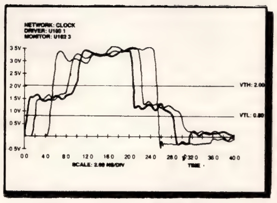

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MOTIVE, the MOdular TIming VErifier, analyzes circuit timing over the full range of manufacturing tolerances in minutes, without test vectors.

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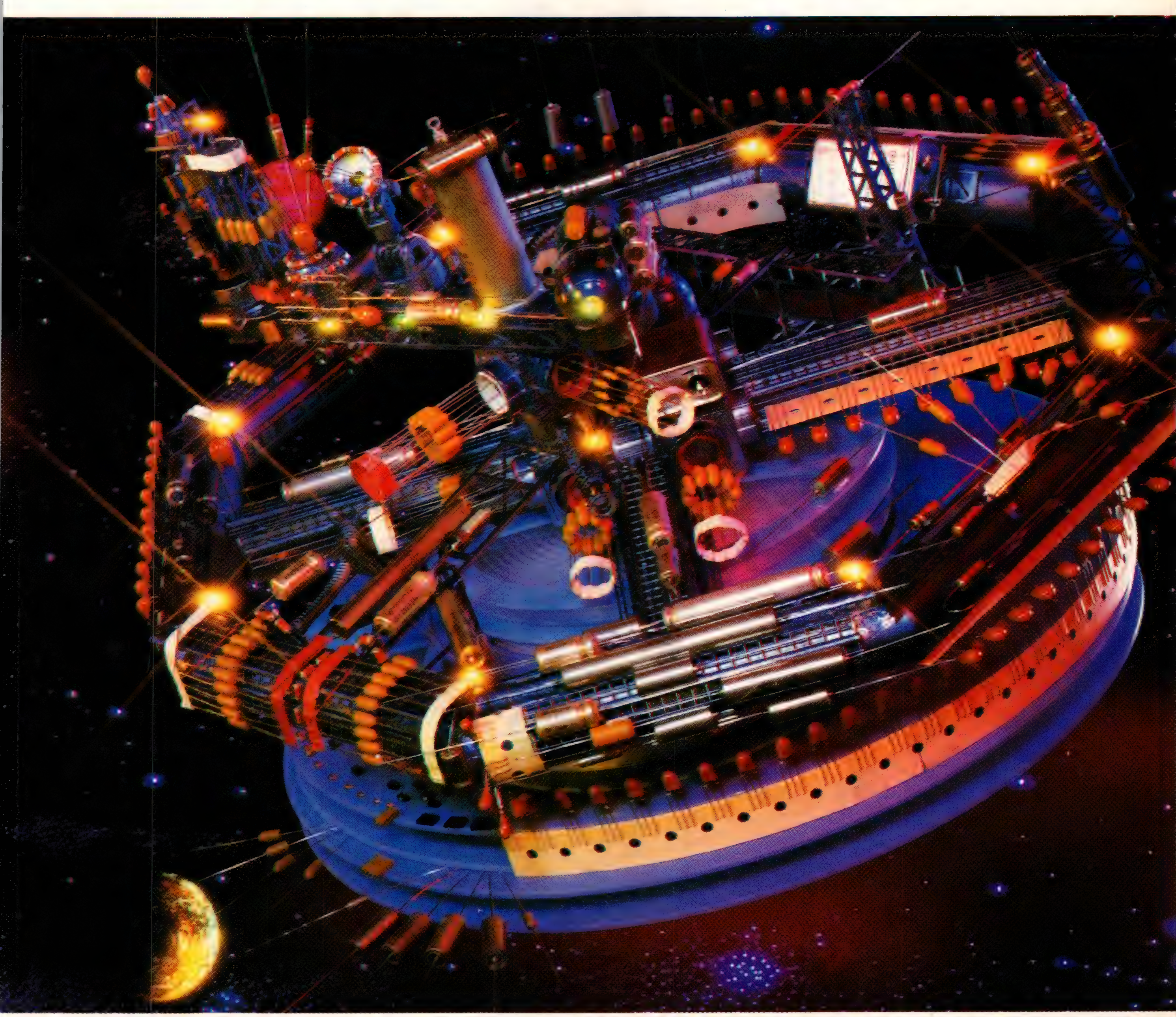
THE TANTALUM PLACE.



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CIRCLE NO 48

RF/MICROWAVE CAE TOOLS

Software programs ease circuit designer's task

RF/microwave CAE tools vary widely in cost and performance. You should make your choice of programs carefully, according to your needs—and the size of your bank account.

Dave Pryce,
Associate Editor

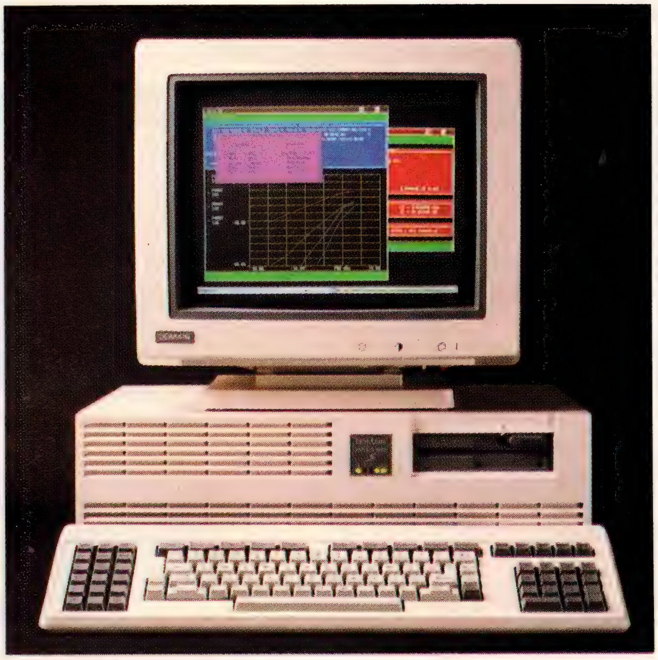
In choosing a CAE software package, you need to consider a program's capabilities in terms of your specific application requirements and—of equal importance—the particular computer on which the software runs. As you might expect, most of the available RF/microwave programs run on IBM PCs, PC/XTs, PC/ATs, and compatibles. For designers that use or prefer Apple computers, however, several programs are available that support the Apple II and the Macintosh.

In many cases, software vendors offer a choice of either personal-computer or workstation programs. In a few cases, only workstation programs are available. Where both are available, the typical workstation-based program is premium-priced compared with its PC-based counterpart. These higher-priced programs generally run on workstations such as those available from Apollo, DEC, HP, and Sun.

Although not as common as CAE tools for digital or low-frequency analog applications, RF/microwave CAE tools are available for a wide range of functions, and at prices ranging from less than $100 to over $30,000. From schematic capture to simulation and analysis to artwork generation and layout, there is likely a CAE software program that will satisfy your needs. And the truly affluent can take possession of a complete hardware/software package that will shrink a bank account by $75,000 to $150,000.

Low-cost programs are useful

Starting at the low-end of the price scale (under $1000), you'll find software packages from BV Engineering, Etron RF Enterprises, and Nedrud Data Systems. These programs peform such functions as microstrip design, attenuator design, filter design, resonant-circuit design, network analysis, and high-resolution graphics.



Capable of performing schematic capture and linear and nonlinear simulations, *the MMIC Design Workstation from EEsof also provides circuit-driven and custom layouts as well as design verification.*

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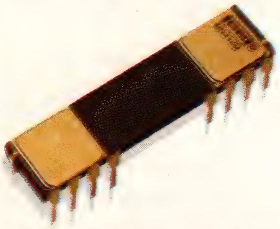
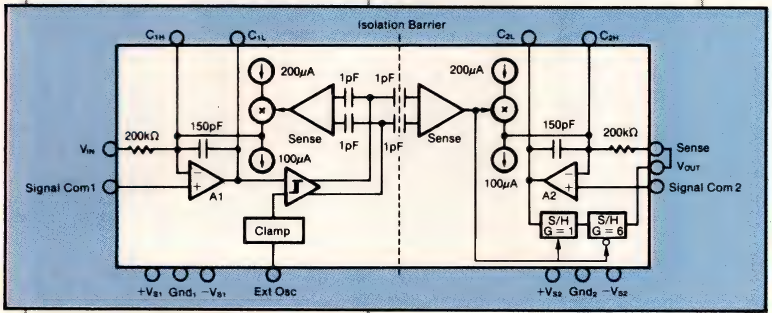
New, Miniature ISO Amp Handles 1500Vrms



Our new ISO120 isolation amplifier gives circuit designers more circuit protection, accuracy, and reliability than ever before possible at such low cost. Its small package, high performance, and low cost are ideal for multichannel data acquisition and industrial control systems and test equipment applications.



Check these features:

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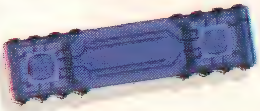

The superior isolation performance of the new amps is achieved using Burr-Brown's revolutionary ceramic capacitive barrier technology, similar to winning designs for the popular ISO102/106 series. The input and output sections of ISO120/121 are galvanically isolated by matched 1pF tungsten capacitors embedded in the ceramic barrier material. This creates a very rugged, completely hermetic isolation barrier able to withstand extreme mechanical, thermal, and electrical stresses with no damage.

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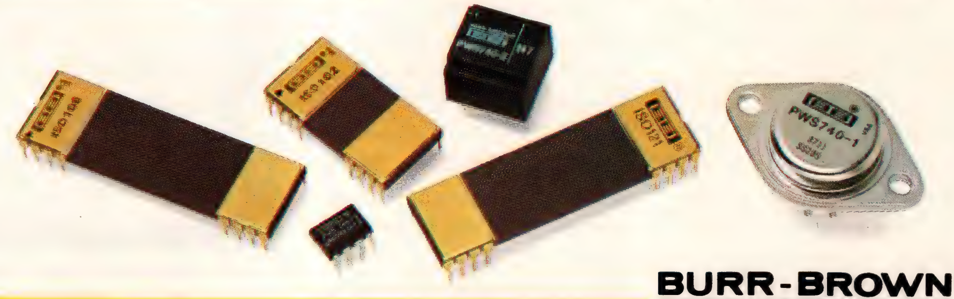

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BB

RF/microwave CAE tools

BV Engineering offers three low-cost programs of interest to RF/microwave designers. The Micro-3 package ($149) is designed for use with the IBM PC and compatibles. It is actually a group of 12 programs that simplifies the design of microstrip line widths and spacing and the establishment of impedances. Several of the programs deal with the design of lowpass, bandpass, and bandstop filters; others handle the design of impedance transformers and directional couplers. In addition to describing program operation, the instruction manual also provides a brief, but informative, history of the methods used to design microstrips.

The other two packages are the LCFIL ($149) and the PCPLOT ($125) programs. LCFIL is a menu-driven program for the design and analysis of passive L-C filters, including Chebyshev, Cauer, and Bessel types. The program covers lowpass, highpass, and bandpass filters, and it computes a filter's gain, phase, and delay characteristics. LCFIL is suitable for lumped-component filters that are realizable to about 400 MHz; it is not intended for use in microwave stripline applications. LCFIL is available in IBM and Macintosh versions.

PCPLOT is a high-resolution graphics program that interfaces with LCFIL and other programs to provide plots of time history, frequency response, and other scientific functions. Template files generated within PCPLOT contain all the physical parameters of a graph such as scaling, area labeling, and file names. IBM, Apple II, and Macintosh versions are available.

Etron RF Enterprises offers a series of low-cost programs on disk (with accompanying instruction booklets) that assist the RF designer in a variety of tasks. All of these RF Notes are written for IBM PC/MS-DOS operation.

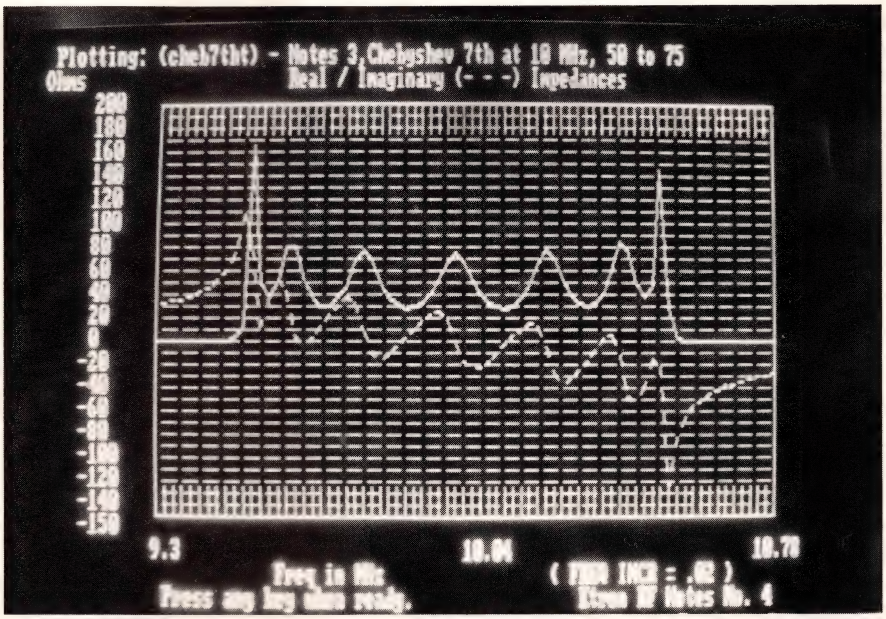

Plotting: (cheb7tht) - Notes 3,Chebyshev 7th at 10 MHz, 50 to 75
Real / Imaginary (- - -) Impedances
Ohms
200
180
160
140
120
100
80
60
40
20
0
-20
-40
-60
-80
-100
-120
-140
-150
9.3
10.04
10.78
Freq in MHz
(FREQ INCR = .02)
Press any key when ready.
Etron RF Notes No. 4

***Fig 1—This screen dump from** Etron RF Enterprise's RF Notes 4 program plots the impedance of a Chebyshev filter that was designed with the RF Notes 3 program.*

RF Notes 1 ($85) covers the design of resonant circuits, striplines, microstrips, and image-parameter filters. It also provides dB/dBm conversion, VSWR analysis, and mixer cross-products evaluation.

RF Notes 2 ($95) is a general design aid that covers the design of attenuator pads, inductors, and impedance-matching networks. It also provides capacitor analysis.

RF Notes 3 covers the design of lowpass, highpass, bandpass, and band-reject filters to the seventh order. It is available in three parts: Vol 1 ($135) covers Butterworth filters, Vol 2 ($135) covers Bessel filters, and Vol 3 ($149) covers Chebyshev filters.

RF Notes 4 ($179) is dedicated to network analysis. Divided into 17 elements and 30 sections, it covers impedance-matching networks, filters, transformers, and transmission lines (including microstrips). The program also features schematic entry and editing, graphics-data output, and the ability to analyze other RF Notes' files and to save design files. **Fig 1** shows a screen dump from RF Notes 4 that plots the impedance of a Chebyshev filter designed with RF Notes 3.

Priced at $980, Dragonwave from Nedrud Data Systems narrowly qualifies for the low-cost category. Dragonwave is designed for use with the Mac and provides a number of features that are useful for microwave design and analysis. Included are noise-figure and stability calculations, microstrip conversion from substrate parameters, a circuit library (with models), and a graphic-entry feature for entering a circuit's topology. The program also writes EEsof's Touchstone files using one of several possible transfer modes, and it has full cut-and-paste capabilities for other programs used for circuits, graphs, and word processing.

Spend more to get more

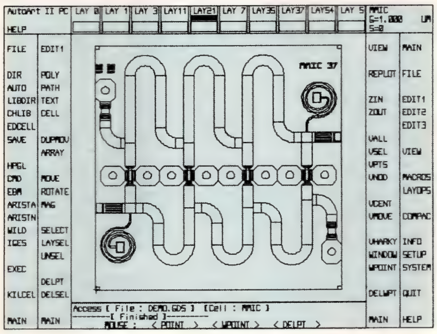
If your bank account is large enough, there's literally dozens of programs from which to choose. Two programs that won't stretch your budget too far are the $1200 RF Designer from ingSOFT Ltd and the $1795 RF Design Kit from Compact Software.

Designed for use with the Mac, the RF Designer provides nodal analysis of 1- and 2-port linear circuits and stability analysis of active circuits. A key feature of the program is its simultaneous optimization of circuit components. The basic package includes a disk that contains s-parameter data for devices from Avantek, Gennum, Hewlett-Packard, Motorola, and CEL/NEC. In addition to the basic package, you can add the RFD Network Analyzer Interface for $250 that supports the HP8753A/B network analyzer, and the Schematic Capture Interface for $250 that formats schematic-capture net lists into the RF Designer's input data files.

The RF Design Kit provides a variety of analysis and synthesis tools and is based on modern analysis and optimization routines for nonlinear systems. The kit includes programs for intermodulation-distortion frequency analysis, noise-figure determination, noise-figure/intercept-point optimization, UHF oscillators, equalizers, and microstrip lines. The Design Kit runs on the IBM PC/XT, PC/AT, and compatibles; the HP Series 200/300; or the HP Series 500.

If your budget can accommodate slightly higher priced products, you may be interested in DGS Associates' S/FILSYN program. S/FILSYN varies in price from $3000 to $5000 and is an interactive filter-design, -synthesis and -analysis program available for personal computers, workstations, and mainframes. The program has been available for over 10 years; according to DGS, it is the one designers turn to for a reliable and capable CAE tool for filter design.

Structured in separate modules, S/FILSYN comes with utilities and script files that enhance its power and simplify its use. The major modules include Passive and Microwave Filters ($5000), Active RC Filters ($3000), and Digital Filters ($4000). A complete program, which includes all of the major modules plus the utilities, costs $10,000. All segments of the various modules can handle lowpass, highpass, bandpass and band-reject filters. Moreover, each of the programs provides full control of all filter characteristics such as flatness, ripple, delay, monotonicity, and symmetry. The prices quoted are for PC-based programs; workstation and mainframe programs cost more.



```
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Fig 2—You can generate a layout of a traveling-wave amplifier *using Compact Software's Autoart II program. Autoart II generates a graphics layout of GaAs monolithic-microwave ICs and millimeter-wave circuits, and it can pass designs directly to plotters and mask-making systems.*

Choose from a variety of programs

Compact Software also has several higher-priced packages that sell in the $3500 to $10,000 range. Over a dozen in number, these programs cover a wide range of RF and microwave functions, including linear and nonlinear analysis, filter design, circuit synthesis, and circuit layout.

The $7500 Supercompact-PC program, for example, is a general-purpose RF/microwave CAD package that provides synthesis, analysis, and optimization for almost any kind of linear circuit from audio through RF and microwave frequencies. The program provides transmission-line synthesis, matching-network synthesis, Monte Carlo analysis, and Smith-chart generation; it also includes s-parameters for over 700 transistors and monolithic-microwave ICs. Supercompact-PC is IBM PC/AT compatible.

A companion to the linear capabilities of Supercompact-PC, Microwave Harmonica ($6000, IBM PC/AT compatible) is targeted for nonlinear circuit simulation and design. The program provides the means to analyze and optimize circuits that operate well into the microwave region. Moreover, because the circuit parameters and current- and voltage-harmonics are optimized simultaneously, nested loops are eliminated, resulting in very fast solutions.

Microwave Harmonica is fully integrated with the Supercompact linear simulator and provides power- and frequency-sweep capability, oscillator analysis, general intermodulation and mixer analysis, and state-of-the-art models of microstrip lines and discontinuities. In addition, the program includes parametric models for FETs, bipolar transistors, and diodes. The company claims that Microwave Harmonica is two orders of magnitude faster than Spice.

Triquint Semiconductor's (Beaverton, OR) MMIC Foundry Library option is also available with either Supercompact or Microwave Harmonica. The MMIC Foundry Library features a user-friendly interactive mode.

Another high-powered program from Compact Software is Autoart II. Identical to the company's Gas Station program (except for the ability to generate EEsof's Touchstone files), Autoart II is a graphics layout package for designing GaAs monolithic-microwave ICs, millimeter-wave circuits, and optoelectronic components. Basically Autoart II is an interactive, 2-dimensional drafting program that translates microwave-circuit descriptions to mask layouts used in fabricating microwave ICs.

The package features a menu-

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oriented and mouse-driven command input, and it provides polygon manipulation, curve generation, automatic generation of Supercompact shapes, and automatic conversion of circuit models to layouts. In the **Fig 2** example, Autoart II has generated a complex FET structure for use in the circuit design of a traveling-wave amplifier. The program is also capable of passing final designs directly to plotters and mask-making systems. An Autoart II PC version costs $5500; a workstation version sells for $10,500.

Hardware is also available

Along with Compact Software, EEsof offers one of the broadest ranges of RF/microwave CAE/CAD programs from which to choose. You can choose from several programs that range in cost from $5000 to over $30,000. The Touchstone program, for example, is probably the leading program of its type. Available in a PC version for $9900 and in workstation versions for $14,000, Touchstone provides linear frequency-domain circuit simulation that tunes, optimizes, and predicts the yield of RF/microwave circuits. Harris Microwave Semiconductor (Milpitas, CA) provides s-parameter-based equivalent-circuit models of its GaAs FETs for use with this program. Touchstone works with Hewlett-Packard and Wiltron network analyzers.

EEsof has many other programs in its catalog. Microwave Spice (PC version, $8800; workstation, $11,500) is a nonlinear time-domain simulation program that simulates the response of microwave circuits to arbitrary waveforms by analyzing the circuit's ac, dc, and transient characteristics. The program includes models for transmission lines and shares common nonlinear device models with EEsof's Libra program.

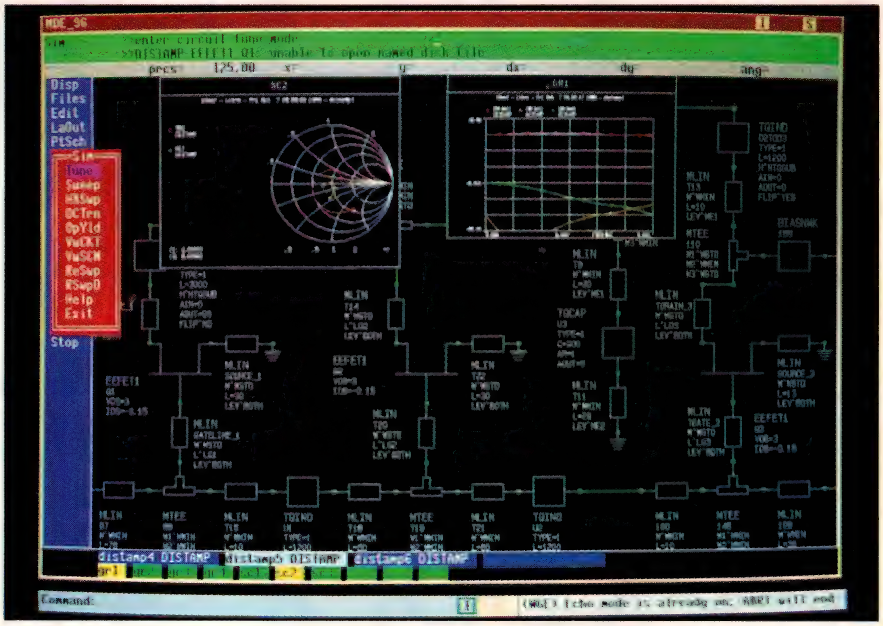

*Fig 3—**Designers can combine this schematic-driven simulation** from EEsof's Academy program with other of the company's programs such as Touchstone and Libra to provide an interactive design environment. You can also use Academy in a layout-driven mode.*

Libra (workstation version available only, $23,000) is a harmonic-balance-type simulator for steady-state frequency-domain simulation. Libra seamlessly integrates Touchstone's linear capabilities and adds power output, distortion, ac waveform, spectral response, and dc analysis of nonlinear microwave circuits. The program also features four large-signal GaAs FET models, including EEsof's bias-dependent model.

EEsof's Academy ($6000, PC; $7200, workstation) is an interface program that works with simulation programs such as Touchstone and Libra to provide an interactive design environment. Schematic-driven simulations (**Fig 3**) as well as layout-driven simulations work within Academy to modify the schematic and layout of a circuit. This bidirectional feature provides added flexibility, thus easing the circuit designer's task.

If price is no object, EEsof also offers a complete hardware/software system that sells for $150,000 and runs on Unix-based Apollo or Sun systems. The MMIC Design Workstation performs schematic entry, linear and nonlinear simulation, circuit-driven and custom layouts, and design verification. It is capable of reading and writing design data to industry-standard formats such as GDSII stream input/output, Libra/Touchstone, and MICAD. The MMIC Design Workstation works with most popular printers and plotters and includes one year of factory support.

Long respected for its sophisticated test equipment, Hewlett-Packard also offers sophisticated software and hardware for the design and analysis of RF/microwave circuits and systems. The vendor's HP-85150A Microwave Design System software, for instance, sells for $29,000. The system features three fully integrated modules. The HP-74210A design-capture module handles schematic entry of a circuit; the HP-85151A module provides simulation and optimization of linear microwave circuits; and the HP-85152A module generates artwork for editing of graphics and the

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CIRCLE NO 51

translation of system schematics into mechanical drawings.

The Microwave Design System software provides extensive capabilities for documenting a design (**Fig 4**). It also links up with other HP electronic- and mechanical-engineering design systems as part of an overall CAE/CAD system called the HP DesignCenter. The HP DesignCenter provides integrated design-automation tools from circuit design through manufacturing and test. The HP-85150A works with the 32-bit HP-9000 Series 300 engineering workstations and the HP-UX operating system, a superset of AT&T's Unix System V.

Hewlett-Packard also offers two completely configured systems that include both the hardware and the software. Each system contains an HP-9000 Series 300 color workstation, the HP-UX operating system, and a hard disk drive (the HP-85150A software is installed at the factory). The $72,950 HP-85150T system uses the Model 350 (4 MIPS) computer; the $47,128 HP-85150E system uses the Model 319C (2 MIPS) computer.

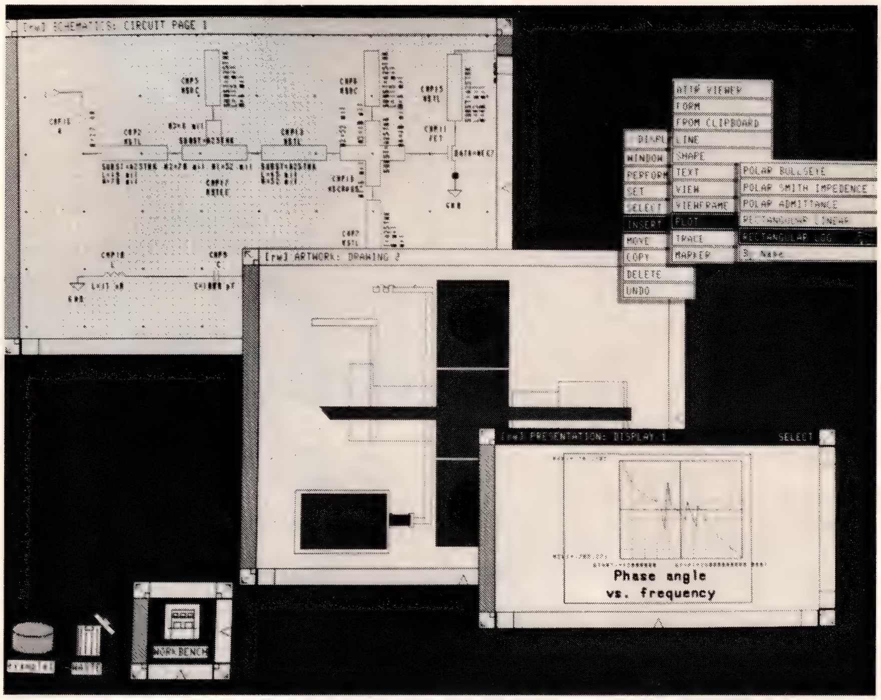

Fig 4—If you need complete documentation capability, *the HP-85150A Microwave Design System software may be just what you're looking for. You can design an amplifier using the software; the program will then generate the schematic, a performance plot, and artwork for circuit fabrication.*

In this brief review of CAE/CAD tools it is obvious that, whatever your needs, there is a software package that will likely fill them. And, with a price range that extends from less than $100 to more than $30,000, one or more of these programs will also likely fit your bank account. EDN

Article Interest (Circle One)
High 518 Medium 519 Low 520

For more information . . .

For more information on the RF/microwave CAE tools discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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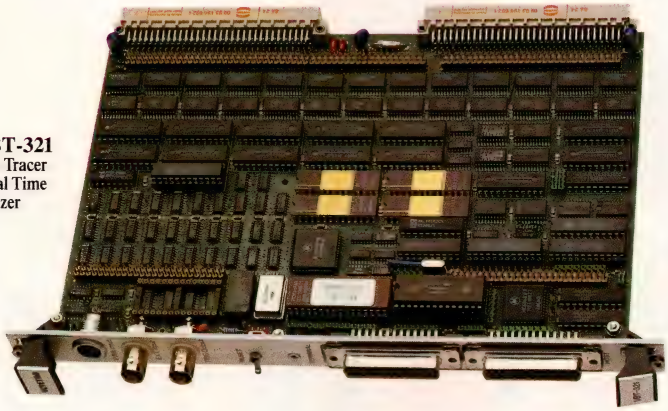

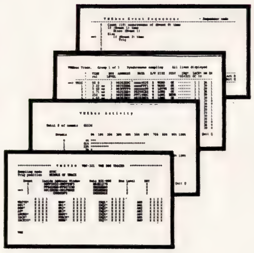

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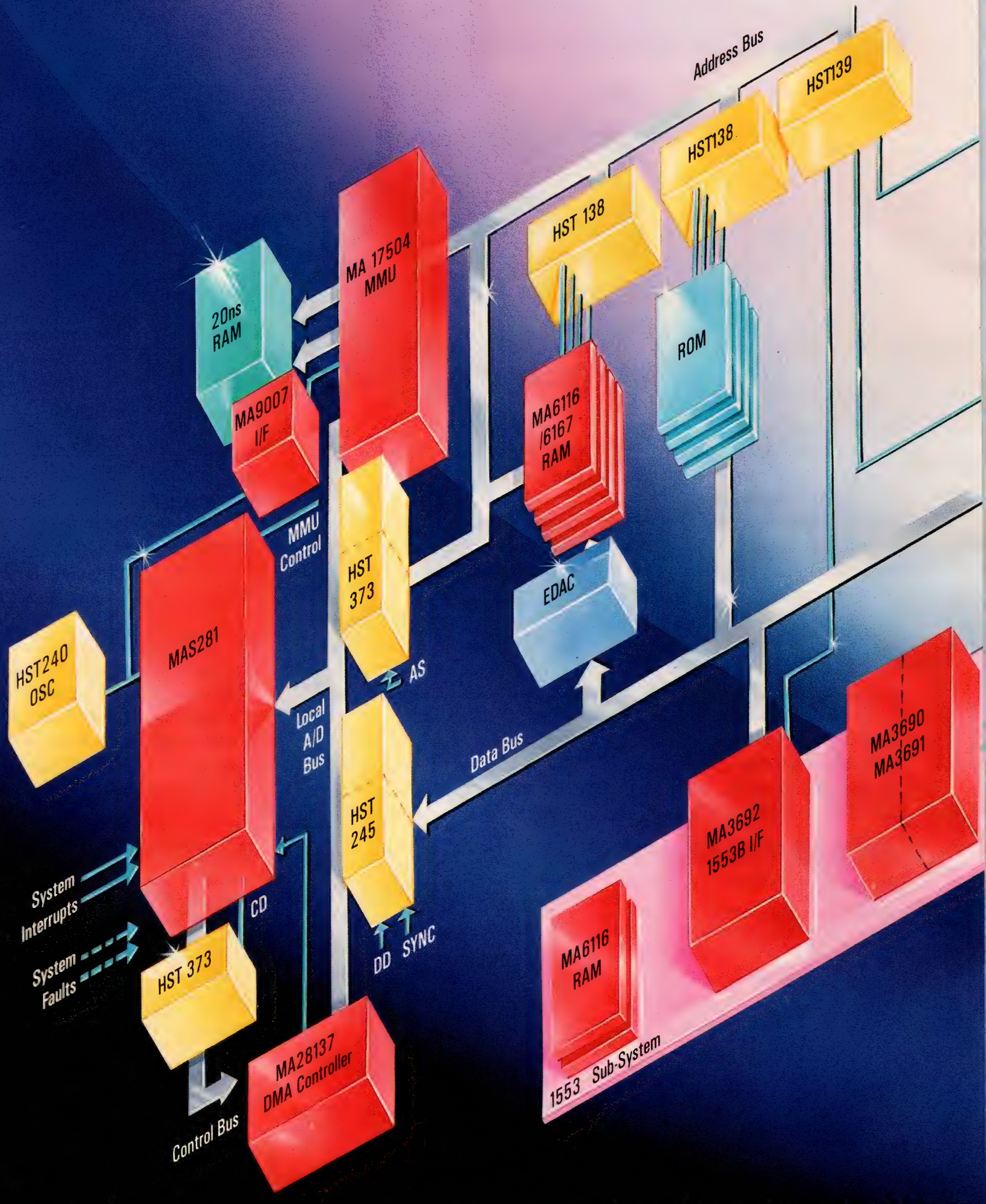
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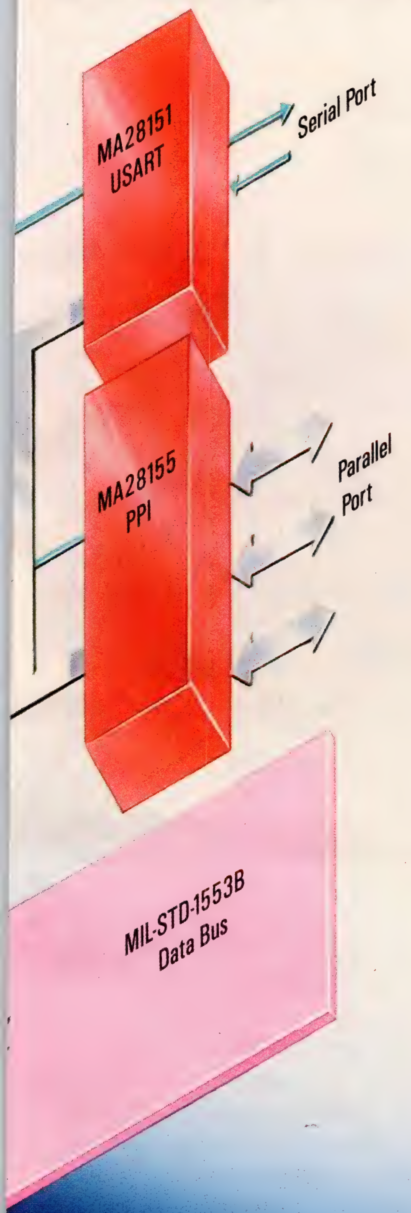

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CIRCLE NO 130

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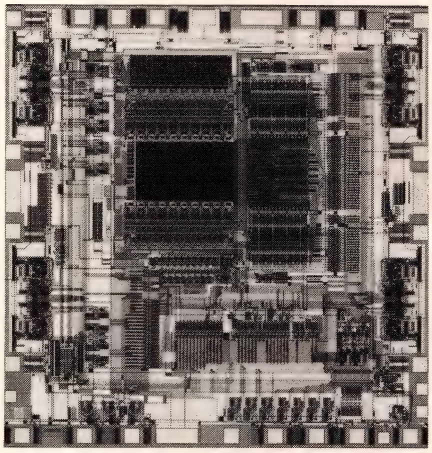
The devices are available in three speed ranges and two power levels. Standard-power 301 devices draw 240 mA; 302s draw 220 mA. Low-power versions of both devices draw only 150 mA. Propagation delay times are 6, 4, or 3 nsec for the 301 and 6, 4, or 2.5 nsec for the 302. The low-power versions are only available with a 6-nsec speed. Both the CY10E301 and CY10E302 are compatible with 10KH series ECL. (Parts numbered CY100E301 and -302 are compatible with 100K series ECL.)

The CY10E301 features 12 input, four input/output, and four output-only signal lines. Each output signal comes from an AND-OR logic combination of the input and output signals or their complements. Each output line also offers selectable polarity, allowing you to specify either high or low as the active logic state. The device is functionally equivalent to an industry-standard 16P8.

The CY10E302 offers eight input and four output signal lines. Output signals are logic combinations of input signals and their complements only; output signals are not available to the AND-OR array. This device is equivalent to the 16P4.

Both devices offer a security feature—a special fuse—that helps protect your design from piracy. While this fuse is intact you can read the fuse pattern to verify that the device has been properly programmed. After the security fuse is blown, however, the pattern can no longer be read.



Equivalent to the 16P8, *the CY10E301 ECL PLD offers propagation delay times as fast as 3 nsec and draws only 240 mA.*

The devices are available in a variety of package styles. You can choose 24-pin ceramic DIPs or 28-pin LCCs for standard-power devices. The low-power versions come in plastic or ceramic DIPs or PLCCs. The 3-nsec CY10E301 costs $55.45; the 2.5-nsec CY10E302 is $66.50 (100). Low-power versions in plastic DIPs cost $37 and $44.35 (100), respectively. Samples are available now and production quantities will be available in the second quarter.

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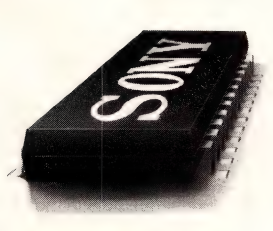

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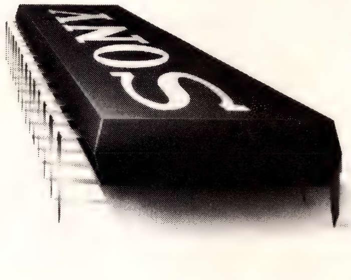

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CXA 1096P	8	BIPOLAR	350mW	DIP
CXA 1096M	8	BIPOLAR	350mW	SOP
CXA 1296P*	8	BIPOLAR	350mW	DIP

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CIRCLE NO 56

Special Report

EDN's advanced CMOS logic ground-bounce tests

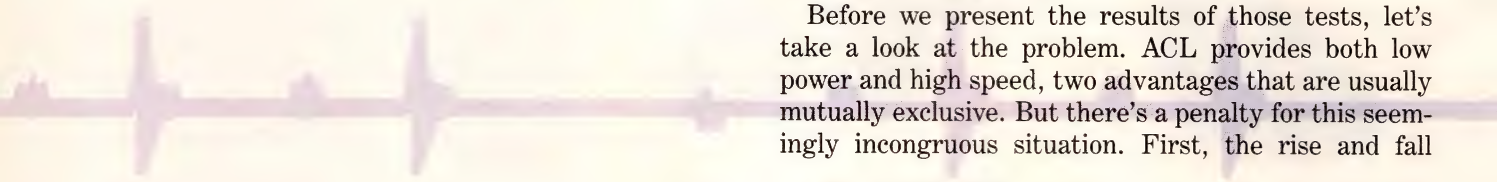
For years, manufacturers of advanced CMOS logic (ACL) chips have squabbled over solutions to the chips' inherent noise problem. Now that ACL chips are widely available in OEM quantities, EDN investigates the issue by running its own ground-bounce tests on chips from five major ACL manufacturers.

David Shear, *Regional Editor*

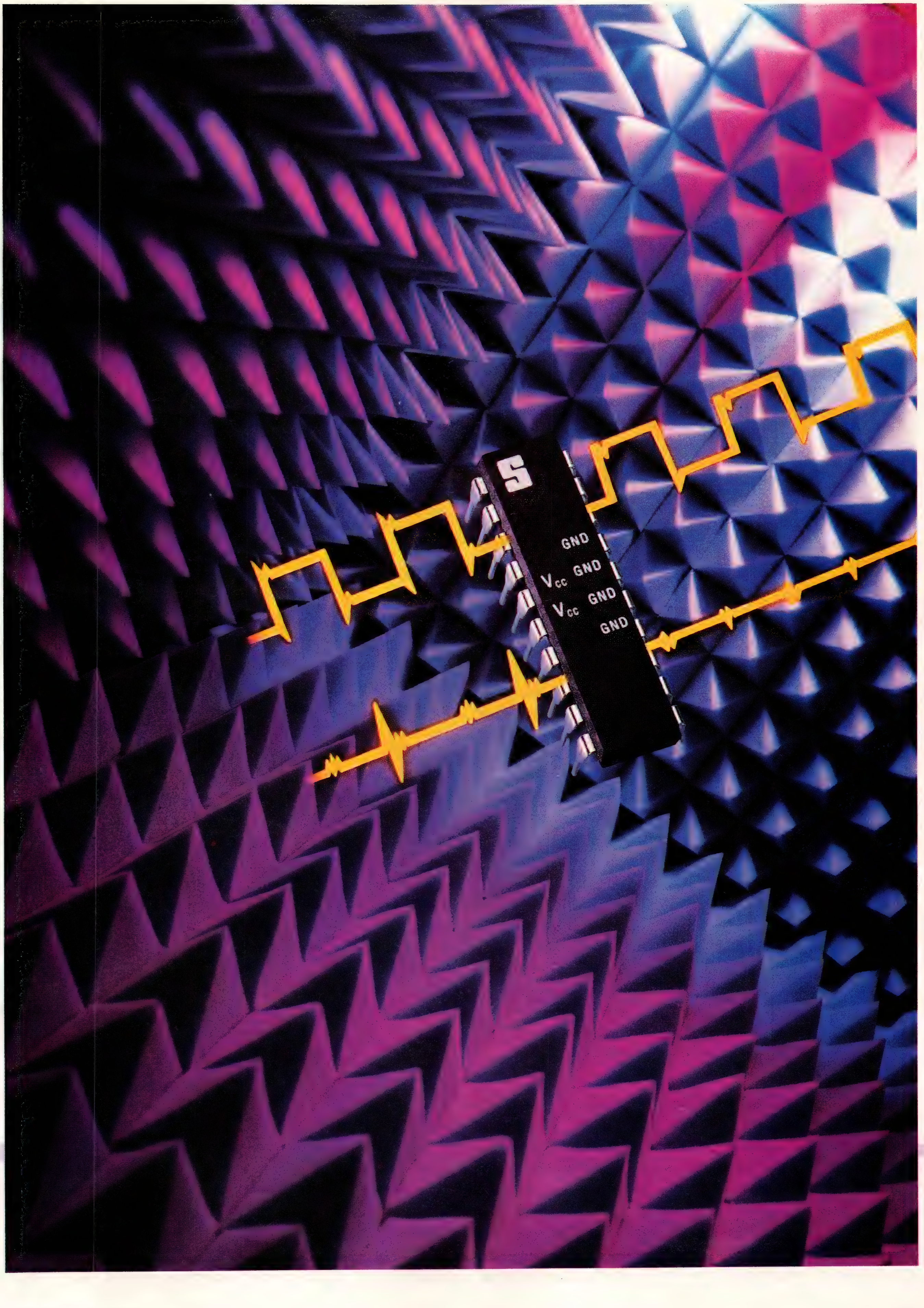
All logic chips are created noisy, but some are more noisy than others. Advanced CMOS logic (ACL) has the dubious distinction of being one of the noisiest logic families. It's also, therefore, one of the most difficult logic families to apply. Manufacturers of ACL chips have addressed this problem in different ways, and each now claims to have the best solution. If you've heard the marketing claims, you might think that ACL no longer has a noise problem. Well, don't let these claims fool you; ACL is still difficult to use.

It's also difficult to choose. Manufacturers offer a bewildering array of specs and data to back up their marketing claims, but they obtain the data by using widely varying test fixtures and methods. To resolve the controversy and assist you in choosing the best ACL chip for your design, EDN conducted its own ground-bounce tests on chips from five major ACL manufacturers. We used the same test fixture and method for all the chips.

Before we present the results of those tests, let's take a look at the problem. ACL provides both low power and high speed, two advantages that are usually mutually exclusive. But there's a penalty for this seemingly incongruous situation. First, the rise and fall



As logic devices become faster, *they become noisier. Manufacturers use a variety of innovative noise-reduction techniques to limit the ground bounce caused by advanced CMOS logic chips. (Photo courtesy Signetics)*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GND
Vcc GND
Vcc GND
GND

ACL provides both low power and high speed, two advantages that are usually mutually exclusive.

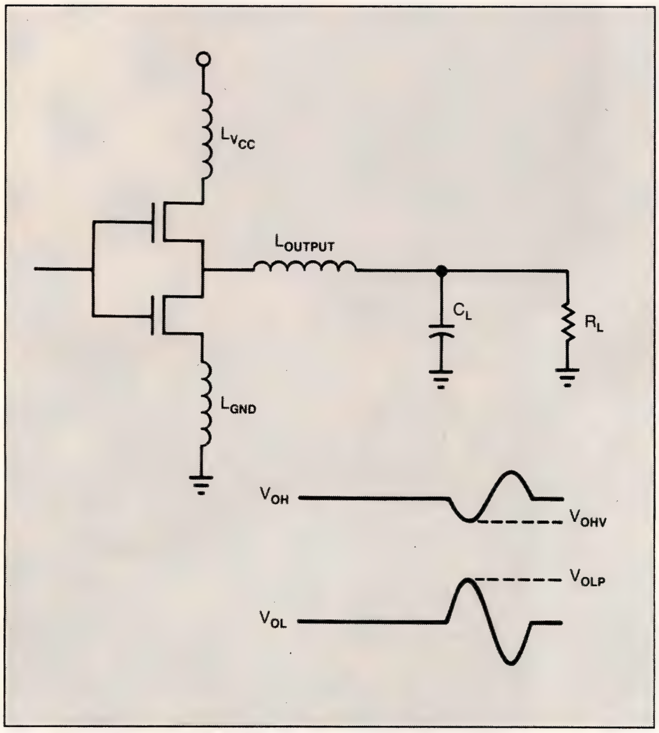


***Fig 1—The inductance on the ground lead (L_{GND})** is a major contributor to ground bounce. As the outputs change level, the current through the inductor changes. This changing current excites the inductor and causes the ground to rise, or "bounce."*

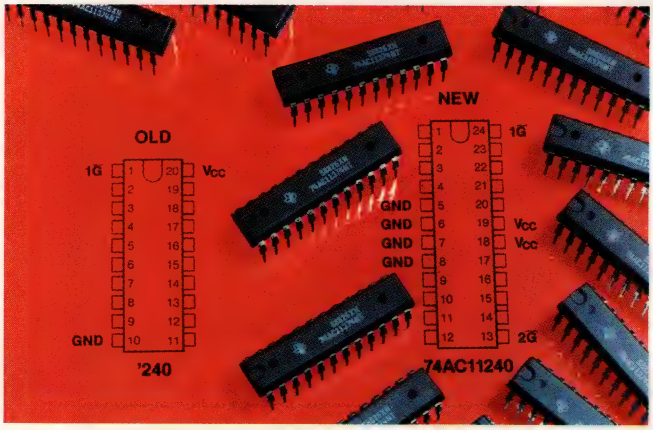


***Fig 2—By moving the V_{CC} and ground pins** to the center of the package, Texas Instruments and Signetics are able to reduce the inductance between the chip and ground.*

times of the outputs are very fast. Also, the outputs must switch between ground and V_{CC} (which is usually 5V), so they require a large amount of current. As the outputs change state, the change in the amount of current that the device draws can be very large. This changing current (di/dt) excites the inductance between the chip and the board, causing the chip's ground to rise, or "bounce" **(Fig 1).**

Ground bounce (also called simultaneous switching noise) can cause a variety of problems. The most obvious occurs when the ground bounce causes an unswitched output to exceed the threshold of the device it is driving: Thus, the driven device detects a logic transition when one is not present. If the unswitched output is driving an edge-sensitive input, the input may falsely clock the device. Such an event can be disastrous. Even worse, it can be nearly impossible to track down. The problem will be intermittent and invisible to most oscilloscopes and many logic analyzers.

Ground bounce also causes input-level shift. As the ground bounces toward a more negative voltage, an input may exceed the device's threshold. For example, if the negative pulse of the ground bounce reaches −2V and the input is at 0.5V, the input is actually 2.5V above ground. The input can register a high logic level, therefore, even though it remains at 0.5V.

Input-level shift, in turn, can cause a latch to lose stored data. If a latch's clock input exceeds its threshold, the latch will store whatever is on its data inputs. In most cases, the inputs will have changed since the latch last stored data. As a result, the original data will be lost, and whatever is on the inputs when the clock's threshold is exceeded will be stored in its place.

Loss of stored data occurs most commonly in situations in which the output of a latch is enabled to be read while it's in 3-state mode. As it's enabled, the output transistors turn on and the ground can bounce, creating a false clock. By the time the data is actually read, the original data may have been lost.

The negative undershoot on an output can also cause trouble. Some of the ACL devices that EDN tested had a negative undershoot of about 2V, which could destroy the input to some RAMs, PLDs, and other devices.

Some engineers believe that any ringing of the output can extend a device's propagation delay. While running the EDN tests, we saw no secondary pulses that exceeded the thresholds. In your system, however, any of the devices we tested has the potential to ring like a bell. However, as long as you observe good design practices, you probably won't have to derate the speed of any of these devices because of ringing.

The package controversy centers around the inductance between the chip and the ground pin, which

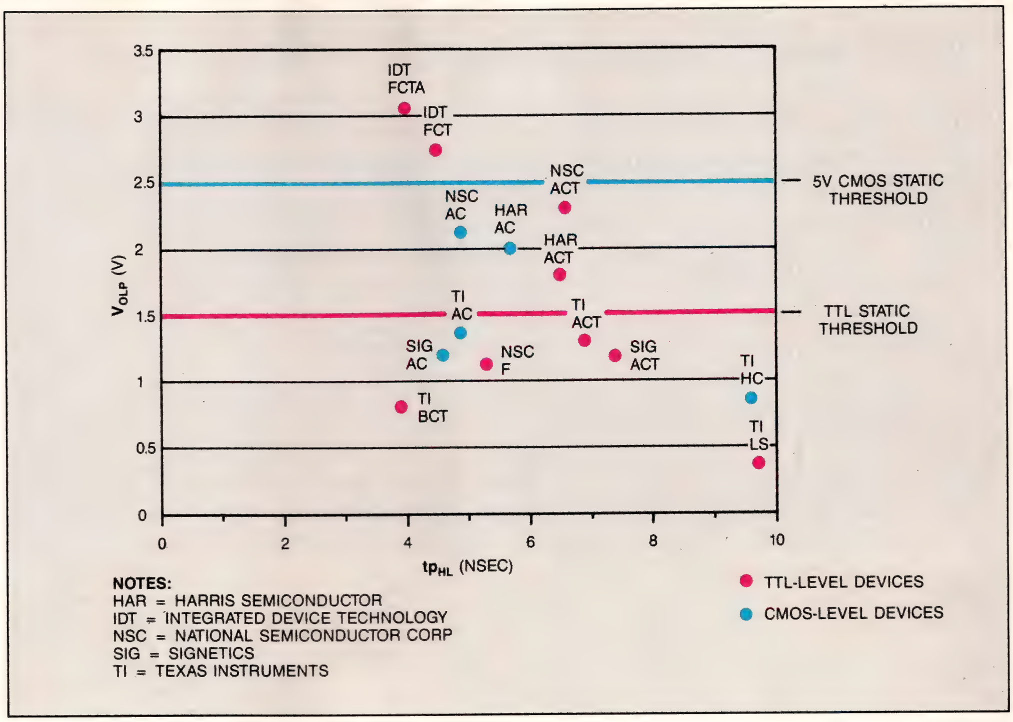


***Fig 3—This plot shows the V_{OLP}** in relation to the propagation delay (tp_{HL}) of all the devices measured.*

causes ground bounce **(Fig 2)**. The traditional end-pin package has an inductance of about 15 nH on the ground lead. The center-pin package has four ground pins in the center of the package and an inductance of about 4 nH. The lower inductance of the center-pin package is supposed to reduce the noise that the device creates. The center-pin package also rearranges the inputs and outputs so that all of the inputs are on one side of the package and all of the outputs are on the other side. This "flow-through pinout" is intended to make it easier to lay out the pc board.

Manufacturers who use center-pin packages for their ACL chips believe that only center-pin packages will limit the noise to an acceptable level. Manufacturers who use the end-pin package claim that these traditional packages do a good enough job of limiting ground bounce. The designer, however, hasn't had access to much objective data on which to base a comparison of the two schemes.

The different test fixtures and methods that the various manufacturers use to test logic devices for ground bounce can give widely varying results. Depending on how you do the test and what fixture you use, you can get very different results from the same part. EDN's test was designed to make a fair comparison of devices in both package types by using similar, electronically equivalent test fixtures. We put a lot of effort into making sure that we used exactly the same test methods for every part we tested. We measured the chips against a common yardstick, so to speak.

To choose a test fixture and method, EDN evaluated those of five major manufacturers of ACL chips—Harris, National Semiconductor, Signetics, Texas Instruments, and Integrated Device Technology (IDT)—and came up with a reasonable compromise. The test fixture and the methods we chose are described in the **box** "EDN's test fixture and methods."

Note that for every part we tested, the manufacturer will give you different values than EDN obtained, because the companies all use slightly different test methods than we did. In fact, there is no absolute value of ground bounce for an ACL chip, and for our purposes, finding such a value was less important than comparing the different products fairly.

All devices have ground bounce

After obtaining the test fixture and determining the test methods, EDN ordered five representative parts from each ACL manufacturer's octal-buffer families (240s). We also ordered several of TI's BCT, LS, and HC parts and National Semiconductor's 74F parts for comparison. We ordered the parts anonymously from distributors. In two cases, as you'll note from the test-result pages (pgs 98 through 114), fewer than five parts were actually delivered to us. In those cases, we only tested the parts we received from the distributors.

EDN tested 14 device families in all. **Fig 3** presents the results of the ground-bounce test on a graph; it shows the ground bounce and the propagation delay for each device family tested. The ground bounce (V_{OLP}) shown is that of the worst-case device of each set we tested. The propagation delay (outputs going from high to low, tp_{HL}) is given for the same device with all seven outputs switching. The figure also shows the devices' static threshold for TTL and CMOS levels.

The ground also bounces when the unswitched output is high. The lowest voltage that the unswitched output reaches because of ground bounce when the output is high is V_{OHV} (voltage output high valley).

Text continued on pg 94

EDN's test fixture and methods

To test the ground bounce of the 14 different types of logic devices, EDN chose to use a modified version of the test fixture described in the Texas Instruments ACL Designer's Handbook. National Semiconductor and Signetics use test fixtures that are very similar to the TI fixture. Our purpose was to come up with a test fixture that would let us compare all of the ACL-family devices as accurately and fairly as possible.

The test fixtures we used (**Fig A**) were based on the fixtures described in the Texas Instruments ACL Designer's Handbook. The pc boards were manufactured by ESH Inc (Tempe, AZ), assembled by Texas Instruments, and modified by EDN.

Each of the outputs has a 50-pF, 500Ω load. The 500Ω resistance is made up of the 450Ω resistor on the board and either a 50Ω termination in the scope or a 50Ω termination in a connector. This method creates a divide-by-10 probe on the test fixture (50/(450+50)). A 50Ω coaxial cable connects the scope to the fixture.

Note that the enable inputs are active low but are not connected directly to ground. For CMOS-level devices, these inputs were held at the test V_{IL} of 1V. For TTL-level devices the TTL V_{IL} of 0V was used. Shorting the enable inputs directly to ground re-

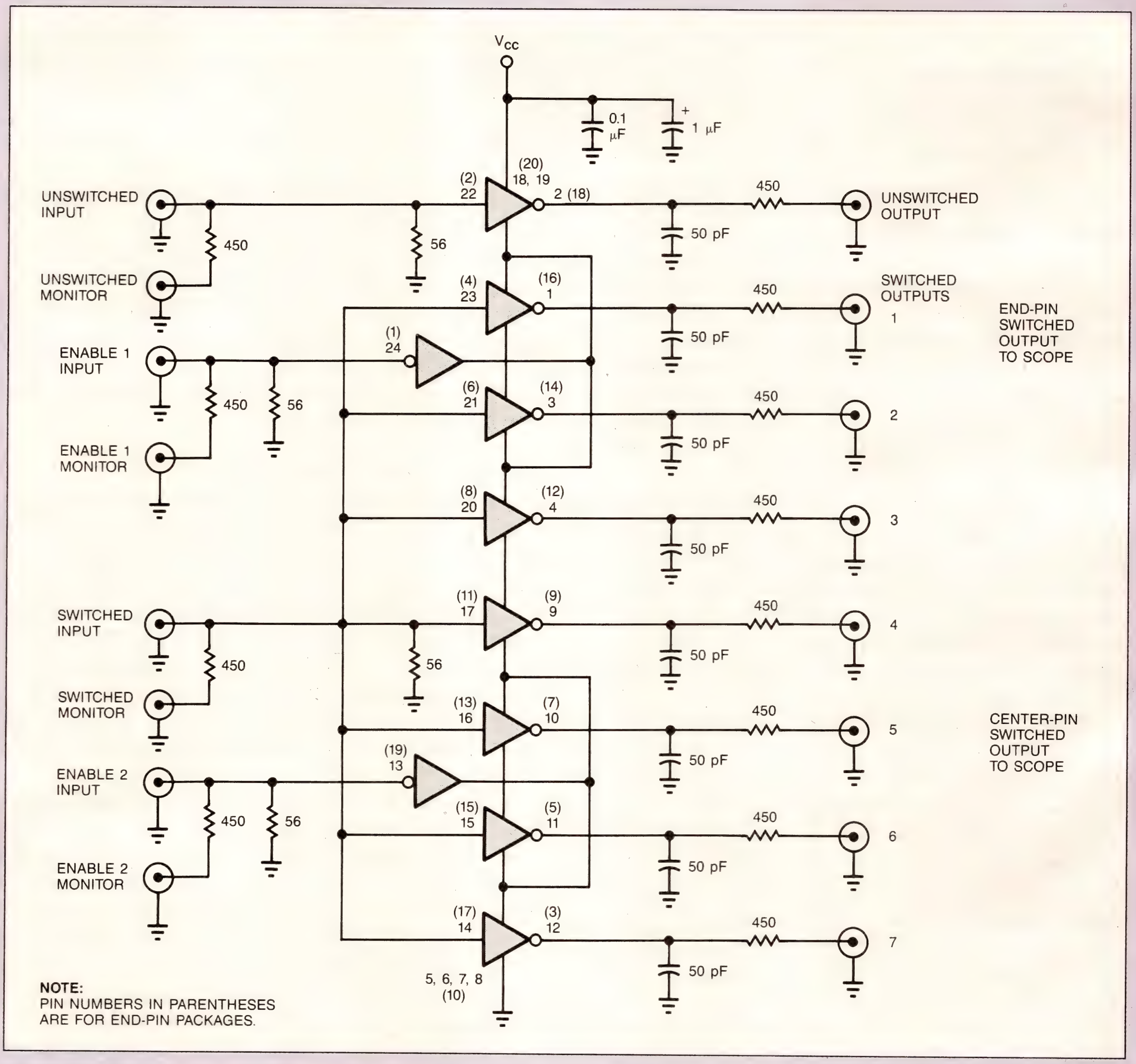


Fig A—***We hard-wired the EDN ground-bounce test fixture*** *to measure the worst-case ground bounce and propagation delay. All of the components of the fixture are surface-mount devices. We used barrel connectors on the test fixture to avoid soldering the devices under test.*

duces the V_{OLP} of some devices by 200 mV. The enable pins allow the current that causes ground bounce to leave the chip by a path other than the ground pin.

The goal of the ground-bounce test was to measure the signal on an unswitched output of an octal inverting 3-state buffer (a 74X240) when all of the other outputs in the package were switching simultaneously. Keep in mind that this procedure is a worst-case test.

The oscilloscope is critical

Fig B shows the test setup. For the tests, we used the Hewlett-Packard 54110D digital oscilloscope. We selected this DSO for its 1-GHz bandwidth, ease of use, and color display. You need a scope with a full 1-GHz bandwidth to take these measurements, because a lower bandwidth will reduce the measured V_{OLP}.

You can use almost any pulse generator, as long as it can generate a 1-MHz square wave, has reasonable rise and fall times (less than 10 nsec) when driving a 50Ω load, and can generate a 0 to 3V and a 1 to 4V signal. We used a Hewlett-Packard 8082A pulse generator.

We used the following procedure to take the measurements that are presented on the result pages.

- Set the unswitched output low
- Set the trigger to positive edge (output going low)
- Measure tp_{HL}
- Measure V_{OLP}(H-L)
- Set the trigger to negative edge (output going high)
- Measure tp_{LH}
- Measure V_{OLP}(L-H)
- Set the unswitched output high
- Measure V_{OHV}(L-H)
- Set the trigger to positive edge (output going low)
- Measure V_{OHV}(H-L)

For CMOS-level devices, $V_{IH}=4V$ and $V_{IL}=1V$. The scope trigger was set to 2.5V and propagation-delay measurements were taken at 2.5V. For TTL-level devices, $V_{IH}=3V$ and $V_{IL}=0V$. The scope trigger was set to 1.5V and propagation-delay measurements were taken at 1.5V.

All of the measurements were taken with the scope display in the normal mode with 5-sec persistence. We took the propagation-delay measurements by setting the start time to 0 and manually setting the stop time to the place where the switched output crossed the appropriate threshold. We took the voltage measurements by manually setting voltage marker 2 to the peak or valley of the unswitched output.

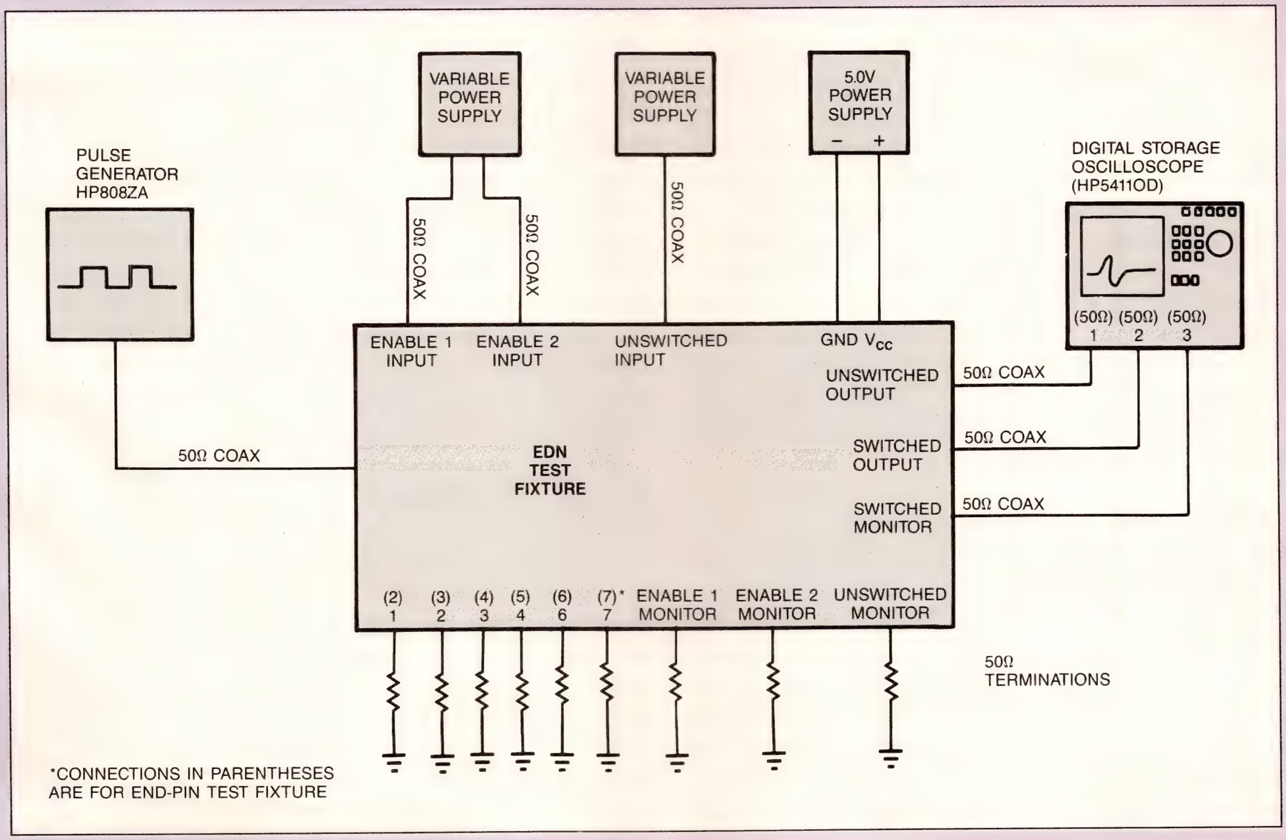


***Fig B—The pulse generator creates the test signal** and the scope monitors the switched and unswitched outputs.*

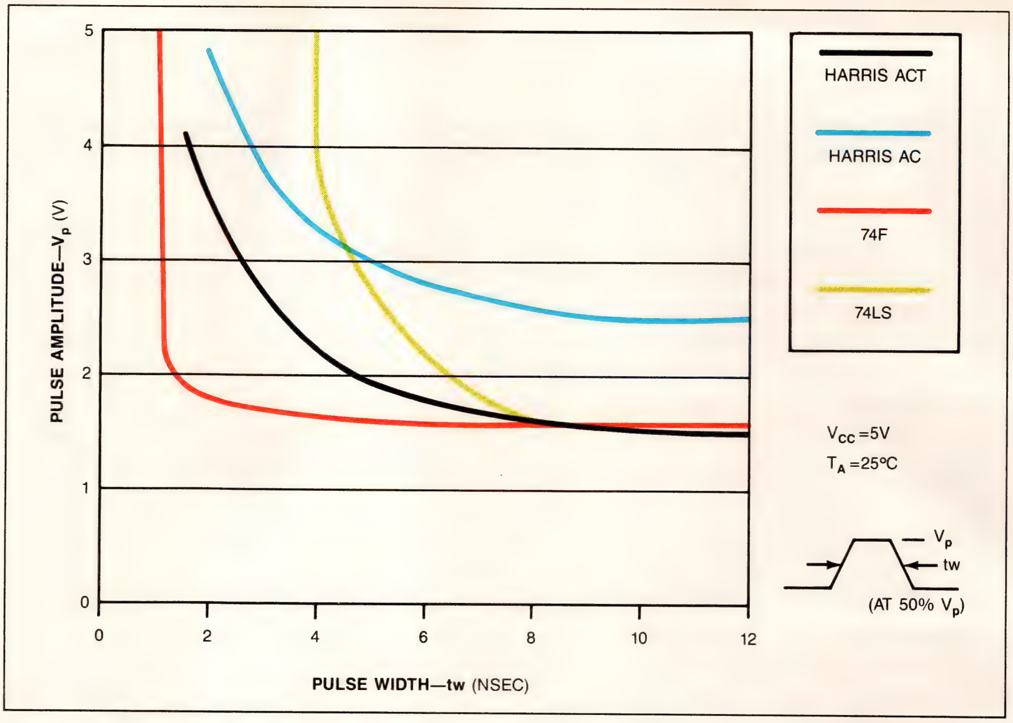


Fig 4—The dynamic threshold of different logic families *shows that a narrow pulse requires a voltage beyond the static threshold in order to be seen by the input. (Data for the 74F and 74LS were supplied by TI. Data for AC and ACT were taken from the Harris ACL data book.)*

The values for V_{OLP}, V_{OHV}, and propagation delay for all of the devices we tested appear in the test results, which begin on pg 98.

When you compare ACL devices' V_{OLP}, you should always compare their propagation delays at the same time. Slower devices usually have a lower V_{OLP}. Also note which pins are being used for the measurement. A V_{OLP} measurement obtained from a randomly selected pin can be as low as half the measurement you'd get from the worst-case pin. The propagation delay can vary by as much as 1.5 nsec. We found that for V_{OLP} the worst-case pins are pin 2 for center-pin packages and pin 18 for end-pin packages. For propagation delay, pin 10 on the center-pin package and pin 16 on the end-pin package gave the slowest measurements.

V_{OLP} also varies with supply voltage and temperature. As the supply voltage increases and the temperature decreases, V_{OLP} increases. We ran all our tests at 22°C and a V_{CC} of 5.0V. The absolute worst case would occur at −55°C and a V_{CC} of 5.5V. However, our comparisons are valid because all the devices were tested under the same conditions.

How much ground bounce is too much?

From the test results we gathered, you might conclude that if you're using the devices we tested to drive a CMOS-level input, the ground bounce of all of the devices, except those from IDT, are below the static threshold. Further, you might conclude that when driving TTL-level devices, all of the center-pin devices will be below the static TTL threshold and all of the end-pin devices will be above the static TTL threshold. If you look no deeper, you may conclude that the center-pin package is the only one to use.

A ground-bounce pulse is not static, however; it's dynamic. **Fig 4** shows some typical dynamic thresholds of three TTL-level logic families and one CMOS-level logic family. The dynamic threshold shows, for a given pulse width, how large the pulse must be in order to be detected at the input. As the pulse narrows, a higher voltage is required to trigger an input. As you can see in the scope photos in the test results, the pulse width of the ground-bounce pulses obtained during the tests is between 3 and 5 nsec.

A pulse of such width must be about 2V to falsely trigger an ACT input and about 3V to trigger an AC input. For 74LS logic (low-power Schottky TTL), the pulse would have to be about 2.8V. But, for 74F devices (advanced Schottky TTL), the pulse would only have to be 1.6V. You must determine which logic family you will be driving before you can evaluate the amount of V_{OLP} your system will be able to withstand. For example, a worst-case test for the ACL parts would be to have an ACL device drive a 74F device, which has a 1.6V dynamic threshold. In that test, all of the end-pin devices that EDN examined failed.

Our V_{OLP} measurement is a worst-case measurement. We used the worst-case pin for each device with a 50-pF, 500Ω load. A real system has a lower and distributed load, which will tend to spread out the pulse. On the other hand, your system will undoubtedly add some inductance from the package to ground, thus adding to the V_{OLP}. The ground-bounce results you see in your system, therefore, could be the same as the worst-case results we obtained in the EDN ground-bounce tests. In fact, the chips could exhibit even worse performance, depending on how much noise your system adds.

So what do you do with all this information? You've seen the results of EDN's ground-bounce tests—we've

Some of the ACL devices EDN tested had a negative undershoot of about 2V, which could destroy the input to some RAMs, PLDs, and other devices.

come up with a value for each part. Just knowing the ground-bounce information for a particular part isn't necessarily going to give you all the information you need to evaluate ACL chips for use in your particular application. In fact, if you focus only on ground-bounce, you're not evaluating all of the data elements that might make up your decision about which circuit to choose. You actually need to have a lot of other key information, most of which is available from manufacturers' data books. For your convenience, the EDN test results contain some of this information for each of the devices tested.

Grounds have always bounced

Ground bounce is not new. It has been around as long as there has been logic. It is largest in ACL, but it does exist elsewhere. For years, you've been using logic that has some amount of ground bounce. We tested 74LS240 and 74HC240 devices for comparison, using the same 50 pF, 500Ω load. The 74LS240 had a V_{OLP} of only 0.34V and the 74HC240 had 0.84V. These low levels indicate why ground bounce has not been a problem for designers who haven't used any of the higher-speed devices. In fact, you would be better off to use the slowest logic family you can get away with. Your design will be much simpler and the noise will be less.

Look at the power consumption

If you look only at ground bounce, you'll find that the 74F family is a little better behaved than the ACL families. But note that the 74F parts consume much more power. The power consumption of a 74F240 is 495 mW. A 74AC240 (or 74AC11240) consumes only 0.44 mW when static, but its power consumption increases as the switching speed increases. At 1 MHz, the 74AC240 consumes 15 mW; at 10 MHz, it consumes 140 mW.

Texas Instruments' 74BCT family is based on a combined bipolar/CMOS process. This family combines the low power of CMOS with the higher drive and better behavior of bipolar outputs. A 74BCT240 consumes

Future ACL chips will feature lower noise

Manufacturers of end-pin packages continue to improve their devices. EDN had an opportunity to test some samples that will be available during 1989. In all cases, the V_{OLP}s of these devices were lower than those of the equivalent devices we purchased and tested for this article.

National Semiconductor is making major modifications to its Fact family and plans to introduce a low-noise version of Fact. The outputs will have a graduated turn-on similar to the output edge control from TI and Signetics. The outputs will also have an undershoot sensor/corrector that will monitor the voltage at the drain of the lower transistor and, if it drops below ground (undershoots), a current injector will supply current to provide a gently decaying load current. The manufacturer intends to use this scheme to reduce undershoot on the output. To minimize the noise at the input section of the chip, the manufacturer put two grounds on the chip, one for the output and another for the input. These grounds remain separate almost all the way to the ground pin (the ground lead looks like a Y). The inputs will also have added hysteresis to improve the input threshold stability.

Harris has modified its parts by using two bonding wires between the chip and the package to reduce some of the ground inductance. The firm is also grading the devices for ground bounce on the basis of the on-resistance of the output drivers. Harris is also planning to introduce an FCT family that will have an I_{OL} of 64 mA (−40 to +85°C). The output does not swing the full 0 to 5V, but is limited to 0 to 3.7V. This limited output swing allows for a slower rise and fall time while maintaining the device's high speed, and it will probably result in a lower V_{OLP}.

IDT is also coming out with a new version of its FCT family; the company limits the output voltage to 3.2V to reduce noise.

Although we tested these and other samples that companies sent us, we didn't include the results in this article. We've provided results only for typical parts that *you* can buy off the shelf today. Mixing purchased parts and selected samples would have yielded an unfair comparison of the devices that are available now.

The lower inductance of the center-pin package is supposed to reduce the noise that the device creates.

391 mW when active but only 66 mW when in the 3-state mode. Since many systems are made up of subsystems on a bus, only one subsystem will be active at a time. As a result, the bipolar/CMOS devices save a considerable amount of power in comparison with bipolar devices.

The 74BCT family uses an end-pin package. Because bipolar outputs are better behaved than ACL outputs, the package inductance is not as great a concern. Refer to **Fig 3** and the test results for further information on this family. In the future, you can expect other manufacturers to bring out bipolar/CMOS bus-driver families that are similar to the Texas Instruments 74BCT chips.

Another contributor to power consumption in ACT devices is the voltage on the input. If the inputs are at 0 or 5V, the quiescent power that the devices consume is very low (0.44 mW). The ΔI_{CC} specification tells you how much extra quiescent current the device requires for each input that is at a voltage typical of the voltage that a bipolar TTL device will deliver (3.4V). For example, the quiescent power consumption of the Harris CD74ACT240E can go from 0.44 to 124 mW if all eight inputs are at 3.4V instead of 5V. The TI and Signetics 74ACT1120s go from 0.44 mW to 44 mW under the same conditions.

The test results provide power-consumption numbers for each of the devices tested. We calculated the power consumption when the devices were static and also when they were switching at 1 MHz and 10 MHz for a square wave. The calculations were made with 50-pF loads on all of the outputs and a V_{CC} of 5.5V. The ambient temperature was −40 to +85°C.

You can't get something for nothing

ACL devices may look as easy to use as 4000 Series CMOS parts (which are very quiet and have high noise margins), but they're not. ACL devices are fast but don't consume lots of power. They may even fit into the same sockets you've been using for years. But the uninformed had better beware—if you don't use ACL devices correctly, you could end up with a very noisy system.

For example, you can't upgrade a slow system to an ACL system without redesigning it. You can't just drop higher-speed logic circuits into your existing low-speed system and expect them to work. If you want to use higher-speed logic properly, you must address a number of concerns that you probably never considered when you created lower-speed designs. At high switching speeds, wires aren't just wires, they're also transmission lines. Outputs aren't just outputs, they're also RF transmitters. Noise can render your system inoperable or make your system fail required RFI and EMI tests.

With proper design methods, however, you can tame noise. To make sure you're designing properly with ACL, unless you're an expert, you should read ACL manufacturers' application notes before you begin. Manufacturers and high-speed-logic designers have made available a veritable mountain of application information for high-speed logic design.

Take a close look at the test results

The scope photos in the EDN test results provide more information than just the level of V_{OLP}. You can also see the undershoot, fall time, and ringing frequency of the output. The undershoot adds to the noise of the system by increasing the voltage range over which the output travels. A 2V undershoot changes a 5V swing to 7V.

Manufacturers of advanced CMOS logic

For more information on advanced CMOS logic chips such as those described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

Harris Semiconductor
Box 591, Mail Stop 432
Somerville, NJ 08876
(201) 685-6562
Circle No 650

Integrated Device Technology Inc
3236 Scott Blvd
Santa Clara, CA 95052
(408) 727-6116
TLX 887766
Circle No 651

National Semiconductor
333 Western Ave
South Portland, ME 04196
(207) 775-8858
Circle No 652

Philips Components
Box 218
5600 MD Eindhoven
The Netherlands
31 40 724173
Circle No 653

Signetics
811 E Arques Ave
Sunnyvale, CA 94088
(408) 991-2531
Circle No 654

Texas Instruments
Semiconductor Group
Box 809066
Dallas, TX 75380
(800) 232-3200 ext 700
(214) 995-6611
Circle No 655

Each manufacturer has its own test fixture and test method; there is no standard. EDN came up with a reasonable compromise.

The fall time can give you an indication of the radiated noise you can expect. An output that quickly switches 7V will produce more radiated noise than an output with a slower fall time that travels 3.2V.

The waveshape and the ringing frequency of the output can be used to verify a test fixture. The output should be a clean, decaying sine wave with a ringing frequency of about 100 to 120 MHz for center-pin packages and 50 to 70 MHz for end-pin packages (**Ref 1**).

When you look at the scope photos on the test-result pages, you will notice that the waveshapes obtained for the IDT devices (especially the 74FCT240AP's) are not very clean. These erratic waveshapes are superimposed on a decaying sine wave, so the V_{OLP} measurement should not be affected. But the erratic shapes do make it difficult to measure the propagation delay. We used the low-to-high propagation delay ($tp_{LH} = tp_{HL}$ on IDT devices) for **Fig 3**'s graph because the falling edge was such a mess.

Limit ground bounce in your system

One way to lower V_{OLP} in your system is to reduce the package inductance. You can do so by using a center-pin package or a surface-mount package. The end-pin SO package has 5 nH of inductance; the end-pin DIP has 15 nH. A surface-mount package may reduce the ground bounce to a more manageable level. We were not able to test surface-mount devices this time because of the complexities the packages would present to the test fixture. In the future, we may be able to test these devices as well. Because there's less inductance in the ground lead of a surface-mount package, these devices will probably exhibit a lower V_{OLP}.

In the design stage, you can also control ground bounce caused by the simultaneous switching of many outputs in one IC. If you don't use an unswitched output to drive a clock input, you may not have a problem with the pulse that the ground bounce creates. You can reduce V_{OLP} by reducing the number of outputs that can switch at the same time. When only three outputs (instead of seven) switched, we saw about a 30% reduction in V_{OLP}.

Within reason, you should always try to reduce noise in your system. If you can reduce a potential noise problem by 700 mV just by selecting a different ACL family, do it. But if you can't fit the larger package into your design, you'll have to use an end-pin device and take greater care to ensure that the noise that the package contributes will not render your system unreliable.

In sum, EDN's tests lead to the conclusion that at present, in the worst case, you can expect an octal device in an end-pin package to have about 700 mV more noise than the same octal device in a center-pin package. Later this year, however, you'll probably see some new end-pin devices that have improved noise characteristics (see **box,** "Future ACL chips will feature lower noise"). But for now, the center-pin devices have the advantage. **EDN**

Acknowledgment

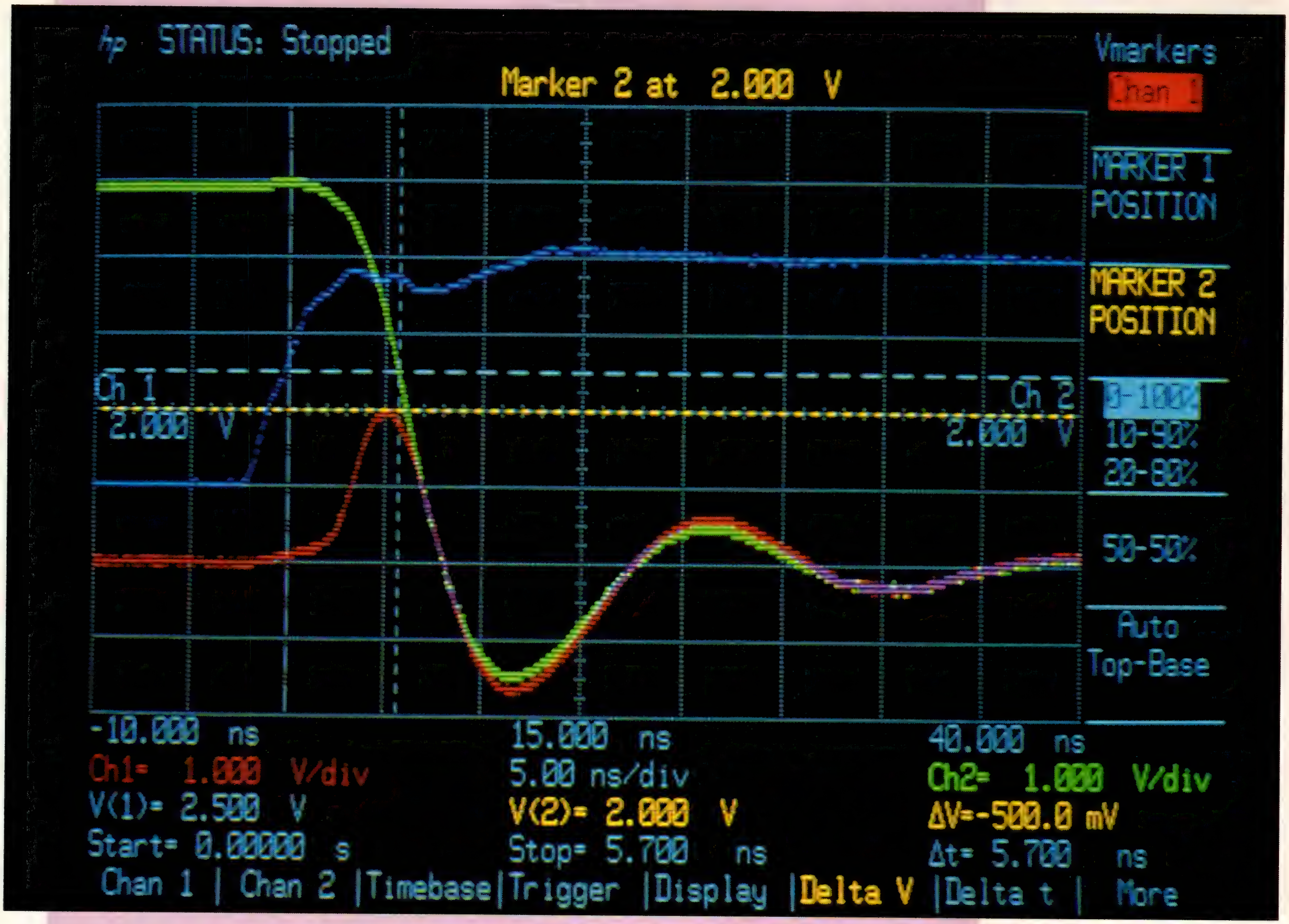
The author gratefully acknowledges the cooperation of the many engineers at Harris Semiconductor, Hewlett-Packard, Integrated Device Technology, National Semiconductor, Signetics, and Texas Instruments who provided information, assistance, test fixtures, and other equipment that made EDN's ground-bounce tests possible. It's not possible for us to list all the names here, but we'd like to extend special thanks to Michael Polacek of Signetics, Dan Powers of Texas Instruments, William Hall of National Semiconductor, and David Grabove of Hewlett-Packard.

Reference

1. Dike, Charles, "Equivalent circuits model subtle traits of advanced CMOS ICs," *EDN*, April 14, 1988, pg 189.

Article Interest Quotient (Circle One)
High 494 Medium 495 Low 496

HARRIS SEMICONDUCTOR CD74AC240E



STATUS: Stopped

Marker 2 at 2.000 V

Ch 1 2.000 V

Ch 2 2.000 V

-10.000 ns

15.000 ns

40.000 ns

Ch1= 1.000 V/div

5.00 ns/div

Ch2= 1.000 V/div

V(1)= 2.500 V

V(2)= 2.000 V

ΔV=-500.0 mV

Start= 0.00000 s

Stop= 5.700 ns

Δt= 5.700 ns

DEVICE	D1	D2
V_{OLP} (V) H-L	2.00	2.00
V_{OLP} (V) L-H	1.44	1.44
V_{OHV} (V) H-L	4.44	4.44
V_{OHV} (V) L-H	3.32	3.32
t_{PHL} (NSEC)	5.7	5.7
t_{PLH} (NSEC)	6.1	6.1
DATE CODE	741	741

TEST CONDITIONS

V_{CC} =5.0V TEMP=22°C V_{IH} =4V V_{IL} =1V

UNSWITCHED OUTPUT PIN=18 SWITCHED OUTPUT PIN=16

DATA-SHEET SPECIFICATIONS

SUPPLY VOLTAGE=1.5 TO 5.5V OPERATING TEMPERATURE=−55 TO +125°C

V_{IH} =3.5V V_{IL} =1.5V I_{OH} =−24 mA I_{OL} =24 mA

POWER DISSIPATION (mW)

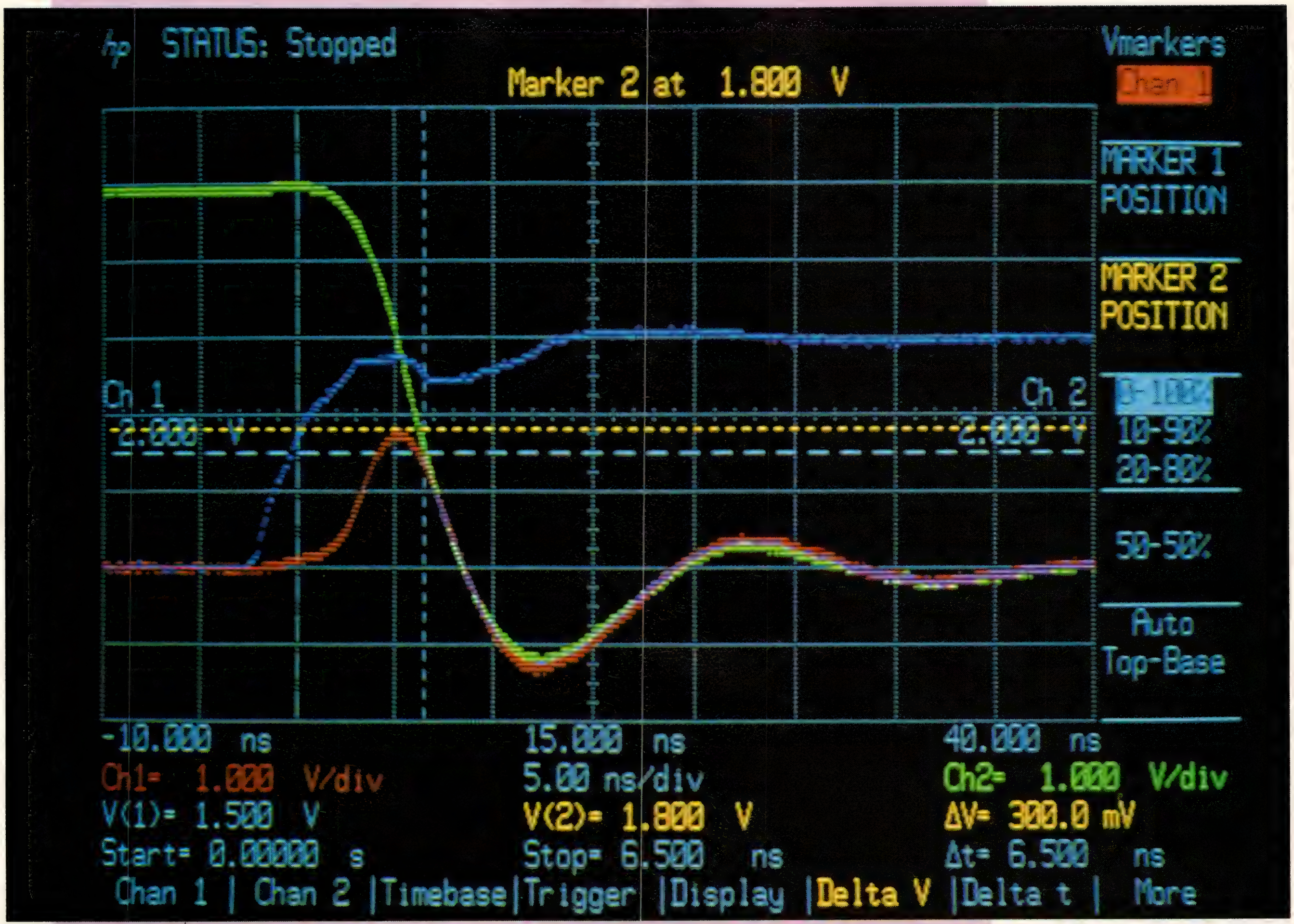
QUIESCENT	1 MHz	10 MHz
0.44	15	141

PROPAGATION DELAY (NSEC)

	TYP	0 TO 70°C	−40 TO +85°C	−55 TO +125°C
t_{PHL}	—	—	6.5	7.2
t_{PLH}	—	—	6.5	7.2

NOTE:
THE SCOPE PHOTO AND THE HIGHLIGHTED COLUMN SHOW THE RESULTS FOR THE WORST-CASE DEVICE.

HARRIS SEMICONDUCTOR CD74ACT240E



STATUS: Stopped

Marker 2 at 1.800 V

Ch1= 1.000 V/div   5.00 ns/div   Ch2= 1.000 V/div

V(1)= 1.500 V   V(2)= 1.800 V   ΔV= 300.0 mV

Start= 0.00000 s   Stop= 6.500 ns   Δt= 6.500 ns

DEVICE	D1	D2	D3	D4
V_{OLP} (V) H-L	1.80	1.80	1.68	1.70
V_{OLP} (V) L-H	1.50	1.50	1.36	1.44
V_{OHV} (V) H-L	4.50	4.40	4.44	4.44
V_{OHV} (V) L-H	3.36	3.38	3.38	3.38
t_{PHL} (NSEC)	6.5	6.4	6.6	6.6
t_{PLH} (NSEC)	6.0	6.0	5.9	6.1
DATE CODE	715	715	715	715

TEST CONDITIONS

V_{CC} =5.0V   TEMP=22°C V_{IH} =3V V_{IL} =0V

UNSWITCHED OUTPUT PIN=18   SWITCHED OUTPUT PIN=16

DATA-SHEET SPECIFICATIONS

SUPPLY VOLTAGE=4.5 TO 5.5V   OPERATING TEMPERATURE=−55 TO +125°C

V_{IH} =2.0V V_{IL} =0.8V I_{OH} =−24 mA I_{OL} =24 mA

POWER DISSIPATION (mW)

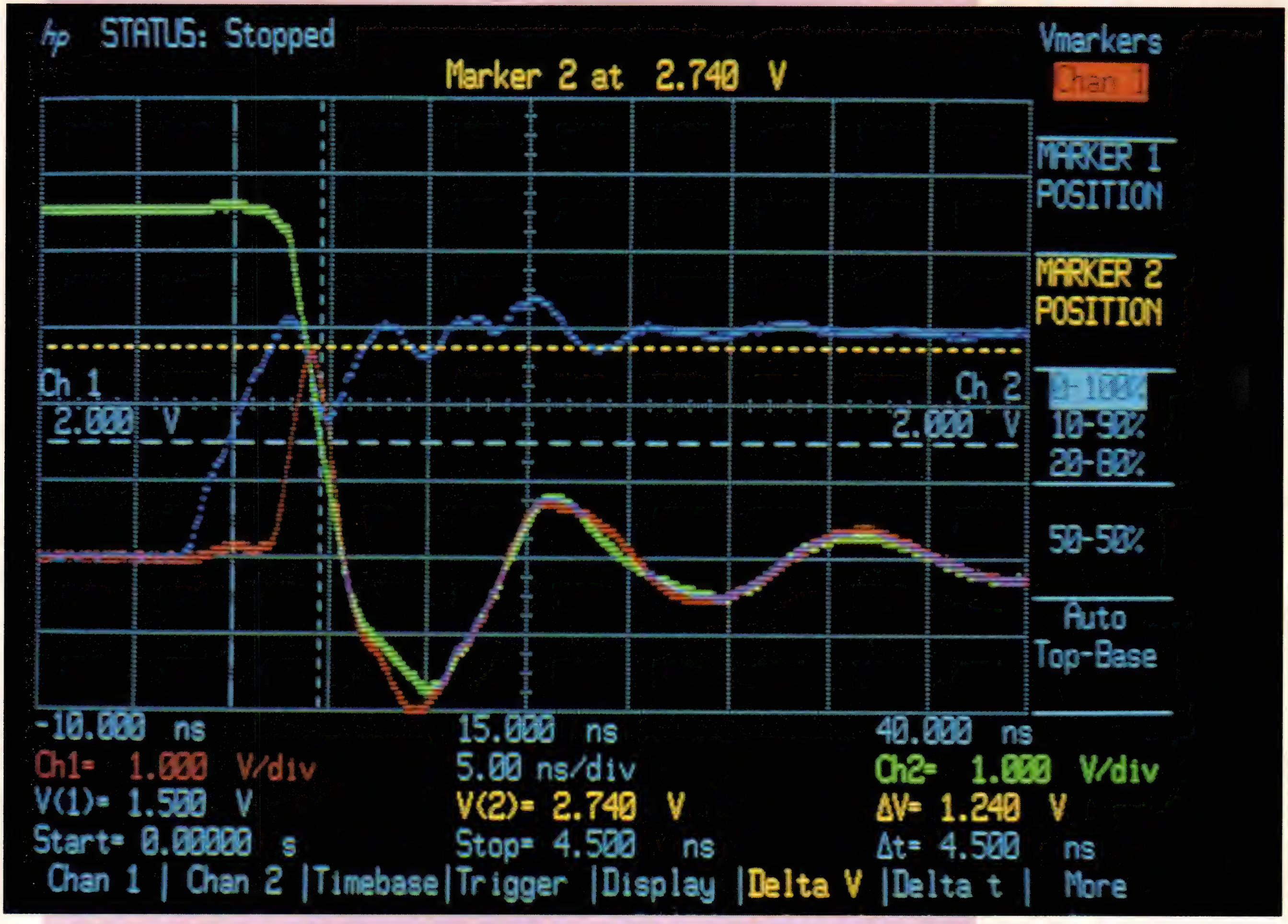
QUIESCENT	1 MHz	10 MHz
0.44 TO 124	15 TO 76	141 TO 203

PROPAGATION DELAY (NSEC)

	TYP	0 TO 70°C	−40 TO +85°C	−55 TO +125°C
t_{PHL}	—	—	7.8	8.6
t_{PLH}	—	—	7.8	8.6

NOTE:
THE SCOPE PHOTO AND THE HIGHLIGHTED COLUMN SHOW THE RESULTS FOR THE WORST-CASE DEVICE.

INTEGRATED DEVICE TECHNOLOGY 74FCT240P



Marker 2 at 2.740 V

Ch1= 1.000 V/div
V(1)= 1.500 V
Start= 0.00000 s
5.00 ns/div
V(2)= 2.740 V
Stop= 4.500 ns
Ch2= 1.000 V/div
ΔV= 1.240 V
Δt= 4.500 ns

DEVICE	D1	D2	D3	D4	D5
V_{OLP} (V) H-L	2.74	2.68	2.74	2.68	2.62
V_{OLP} (V) L-H	1.12	1.18	1.18	1.12	1.12
V_{OHV} (V) H-L	3.94	3.94	3.94	3.94	3.94
V_{OHV} (V) L-H	3.94	3.94	3.94	3.94	3.94
t_{PHL} (NSEC)	4.5	4.6	4.5	4.6	4.8
t_{PLH} (NSEC)	4.7	4.7	4.6	4.7	4.9
DATE CODE	8833FP	8833FP	8833FP	8833FP	8833FP

TEST CONDITIONS

V_{CC}=5.0V TEMP=22°C V_{IH}=3V V_{IL}=0V

UNSWITCHED OUTPUT PIN=18 SWITCHED OUTPUT PIN=16

DATA-SHEET SPECIFICATIONS

SUPPLY VOLTAGE=4.5 TO 5.5V OPERATING TEMPERATURE=0 TO 70°C
−55 TO +125°C (54)*

V_{IH}=2.0V V_{IL}=0.8V I_{OH}= −15 mA
−12 mA (54) I_{OL}=64 mA
48 mA (54)

POWER DISSIPATION (mW)

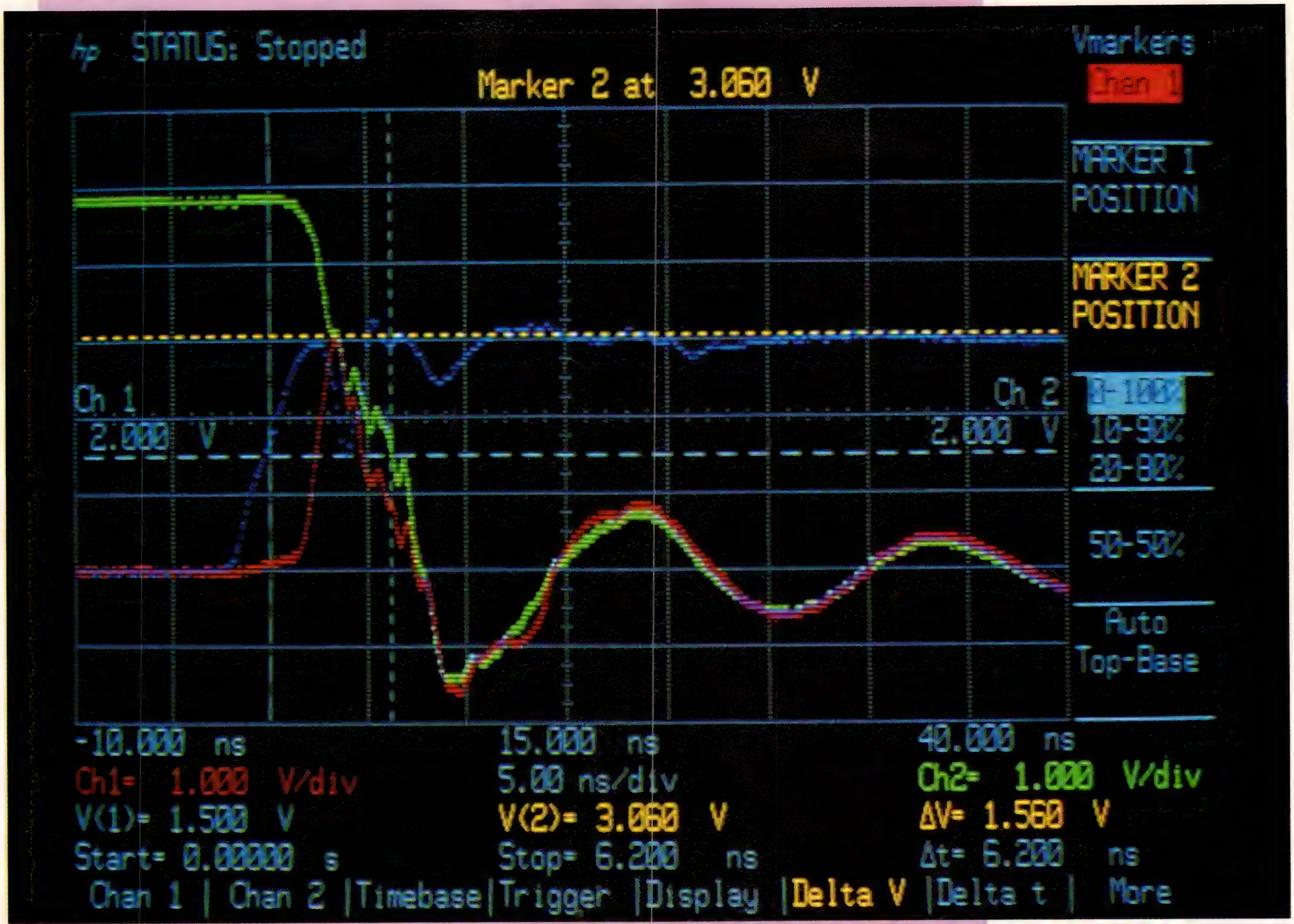
QUIESCENT	1 MHz	10 MHz
8 TO 96	31 TO 75	239 TO 283

PROPAGATION DELAY (NSEC)

	TYP	0 TO 70°C	−40 TO +85°C	−55 TO +125°C (54)
t_{PHL}	5.0	8.0	—	9.0
t_{PLH}	5.0	8.0	—	9.0

NOTES:
THE SCOPE PHOTO AND THE HIGHLIGHTED COLUMN SHOW THE RESULTS FOR THE WORST-CASE DEVICE.
*SPECS LABELED "(54)" ARE FOR THE MILITARY-TEMPERATURE-RANGE VERSION OF THE SAME PART.

INTEGRATED DEVICE TECHNOLOGY 74FCT240AP



```
hp  STATUS: Stopped
                     Marker 2 at  3.060  V
Ch 1                                   Ch 2
2.000  V                               2.000  V
-10.000  ns          15.000  ns             40.000  ns
Ch1=  1.000  V/div   5.00 ns/div            Ch2=  1.000  V/div
V(1)= 1.500  V       V(2)= 3.060  V         ΔV= 1.560  V
Start= 0.00000  s    Stop= 6.200  ns        Δt= 6.200  ns
```

DEVICE	D1	D2	D3	D4	D5
V_{OLP} (V) H-L	3.06	2.94	2.94	2.94	2.86
V_{OLP} (V) L-H	1.44	1.36	1.36	1.36	1.30
V_{OHV} (V) H-L	3.36	3.64	3.76	3.56	3.80
V_{OHV} (V) L-H	3.56	3.64	3.64	3.64	3.70
t_{PHL} (NSEC)	6.2	5.8	5.5	5.9	4.7
t_{PLH} (NSEC)	4.0	4.2	4.2	4.2	4.3
DATE CODE	8833M	8833M	8833M	8833M	8833M

TEST CONDITIONS

V_{CC}=5.0V TEMP=22°C V_{IH}=3V V_{IL}=0V

UNSWITCHED OUTPUT PIN=18 SWITCHED OUTPUT PIN=16

DATA-SHEET SPECIFICATIONS

SUPPLY VOLTAGE=4.5 TO 5.5V OPERATING TEMPERATURE=0 TO 70°C
−55 TO +125°C (54)*

V_{IH}=2.0V V_{IL}=0.8V I_{OH}= −15 mA
−12 mA (54) I_{OL} = 64 mA
48 mA (54)

POWER DISSIPATION (mW)

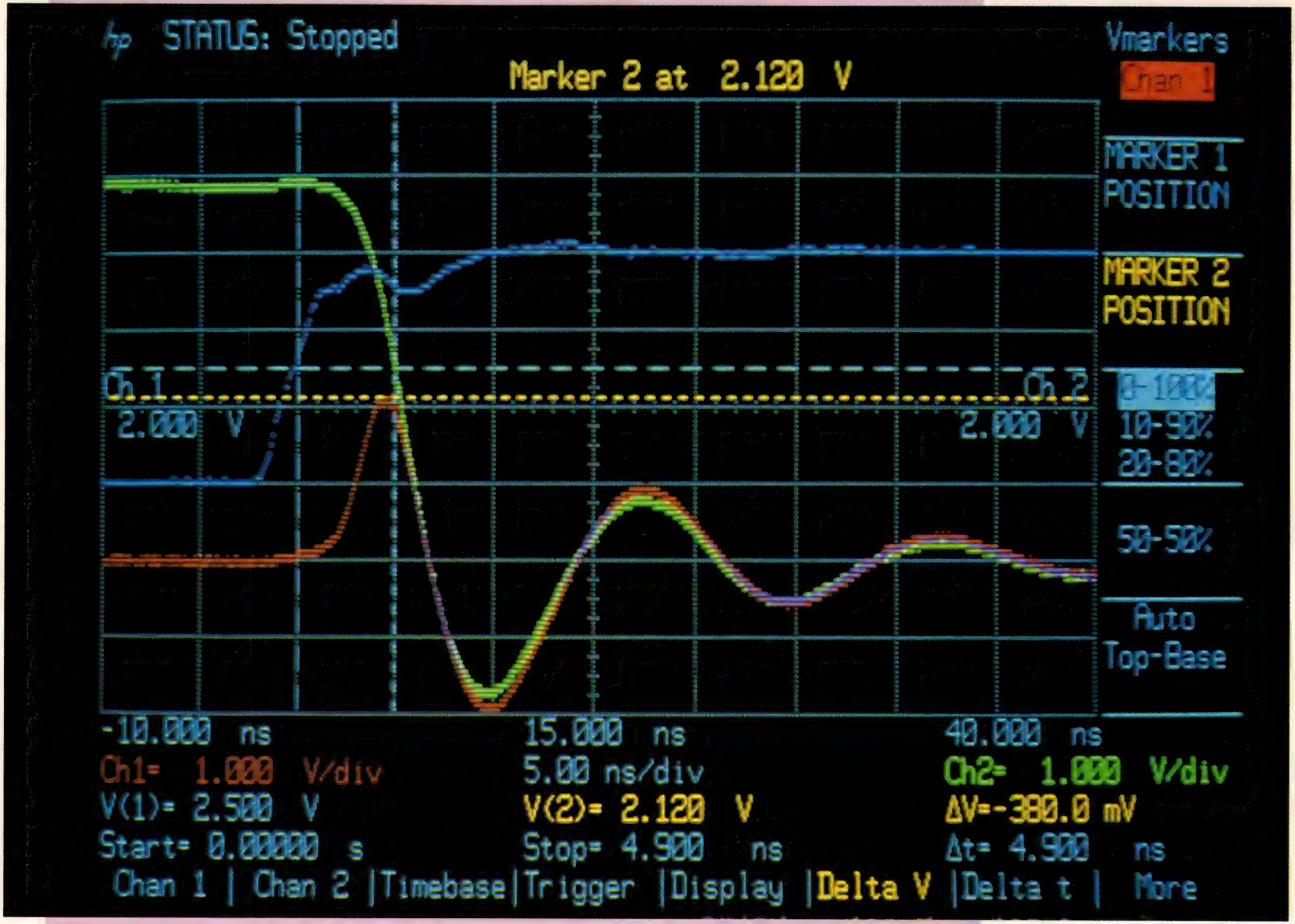
QUIESCENT	1 MHz	10 MHz
8 TO 96	31 TO 75	239 TO 283

PROPAGATION DELAY (NSEC)

	TYP	0 TO 70°C	−40 TO +85°C	−55 TO +125°C (54)
t_{PHL}	3.5	4.8	—	5.1
t_{PLH}	3.5	4.8	—	5.1

NOTES:
THE SCOPE PHOTO AND THE HIGHLIGHTED COLUMN SHOW THE RESULTS FOR THE WORST-CASE DEVICE.
*SPECS LABELED "(54)" ARE FOR THE MILITARY-TEMPERATURE-RANGE VERSION OF THE SAME PART.

NATIONAL SEMICONDUCTOR 74AC240PC



Marker 2 at 2.120 V

Ch 1 2.000 V

Ch 2 2.000 V

-10.000 ns 15.000 ns 40.000 ns

Ch1= 1.000 V/div 5.00 ns/div Ch2= 1.000 V/div

V(1)= 2.500 V V(2)= 2.120 V ΔV=-380.0 mV

Start= 0.00000 s Stop= 4.900 ns Δt= 4.900 ns

DEVICE	D1	D2	D3	D4	D5
V_{OLP} (V) H-L	2.12	2.06	2.06	2.06	2.12
V_{OLP} (V) L-H	1.14	1.12	1.12	1.12	1.18
V_{OHV} (V) H-L	4.44	4.44	4.44	4.44	4.44
V_{OHV} (V) L-H	3.64	3.64	3.64	3.64	3.64
tp_{HL} (NSEC)	4.9	5.1	5.0	5.0	4.9
tp_{LH} (NSEC)	5.3	5.5	5.4	5.4	5.3
DATE CODE	8818	8818	8818	8818	8818

TEST CONDITIONS

V_{CC}=5.0V TEMP=22°C V_{IH}=4V V_{IL}=1V

UNSWITCHED OUTPUT PIN=18 SWITCHED OUTPUT PIN=16

DATA-SHEET SPECIFICATIONS

SUPPLY VOLTAGE=2.0 TO 6.0V OPERATING TEMPERATURE= −40 TO +85°C
−55 TO +125°C (54)*

V_{IH}=3.5V V_{IL}=1.5V I_{OH}=−24 mA I_{OL}=24 mA

POWER DISSIPATION (mW)

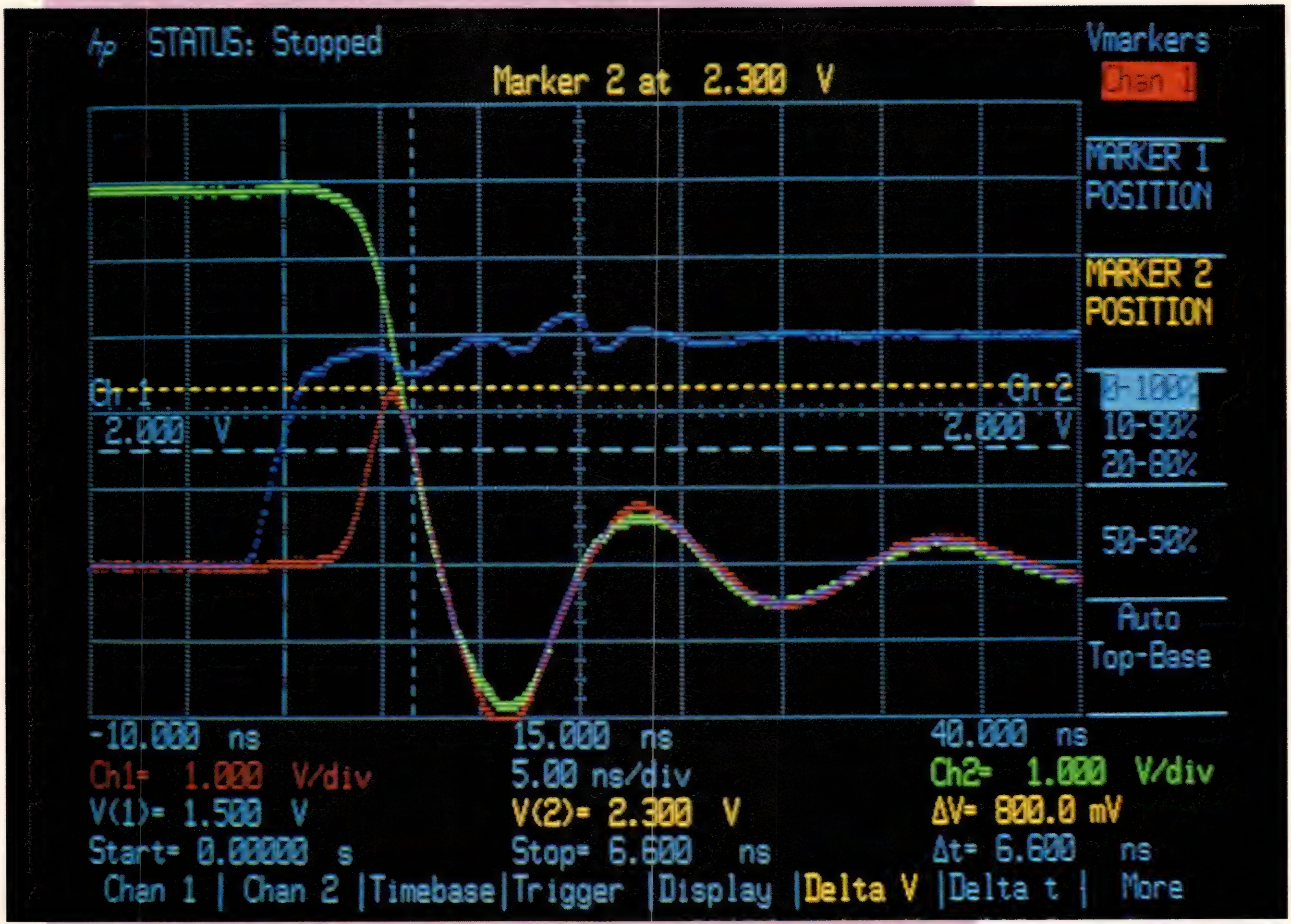
QUIESCENT	1 MHz	10 MHz
0.44	14	135

PROPAGATION DELAY (NSEC)

	TYP	0 TO 70°C	−40 TO +85°C	−55 TO +125°C (54)
tp_{HL}	4.5	—	6.5	8.0
tp_{LH}	4.5	—	7.0	8.5

NOTES:
THE SCOPE PHOTO AND THE HIGHLIGHTED COLUMN SHOW THE RESULTS FOR THE WORST-CASE DEVICE.
*SPECS LABELED "(54)" ARE FOR THE MILITARY-TEMPERATURE-RANGE VERSION OF THE SAME PART.

NATIONAL SEMICONDUCTOR 74ACT240PC



Marker 2 at 2.300 V

Ch1= 1.000 V/div
5.00 ns/div
Ch2= 1.000 V/div
V(1)= 1.500 V
V(2)= 2.300 V
ΔV= 800.0 mV
Start= 0.00000 s
Stop= 6.600 ns
Δt= 6.600 ns

DEVICE	D1	D2	D3	D4	D5
V_{OLP} (V) H-L	2.30	2.30	2.18	2.30	2.18
V_{OLP} (V) L-H	1.18	1.18	1.06	1.18	1.06
V_{OHV} (V) H-L	4.26	4.32	4.32	4.26	4.32
V_{OHV} (V) L-H	3.38	3.50	3.50	3.38	3.56
t_{PHL} (NSEC)	6.6	6.8	5.8	6.5	6.3
t_{PLH} (NSEC)	6.6	6.7	4.9	5.6	5.3
DATE CODE	8620	8620	8734	8620	8734

TEST CONDITIONS

V_{CC}=5.0V TEMP=22°C V_{IH}=3V V_{IL}=0V

UNSWITCHED OUTPUT PIN=18 SWITCHED OUTPUT PIN=16

DATA-SHEET SPECIFICATIONS

SUPPLY VOLTAGE=4.5 TO 5.5V OPERATING TEMPERATURE= −40 TO +85°C
−55 TO +125°C (54)*

V_{IH}=2.0V V_{IL}=0.8V I_{OH}=−24 mA I_{OL}=24 mA

POWER DISSIPATION (mW)

QUIESCENT	1 MHz	10 MHz
0.44 TO 66	14 TO 47	135 TO 168

PROPAGATION DELAY (NSEC)

	TYP	0 TO 70°C	−40 TO +85°C	−55 TO +125°C (54)
t_{PHL}	5.5	—	8.5	9.0
t_{PLH}	6.0	—	9.5	9.5

NOTES:
THE SCOPE PHOTO AND THE HIGHLIGHTED COLUMN SHOW THE RESULTS FOR THE WORST-CASE DEVICE.
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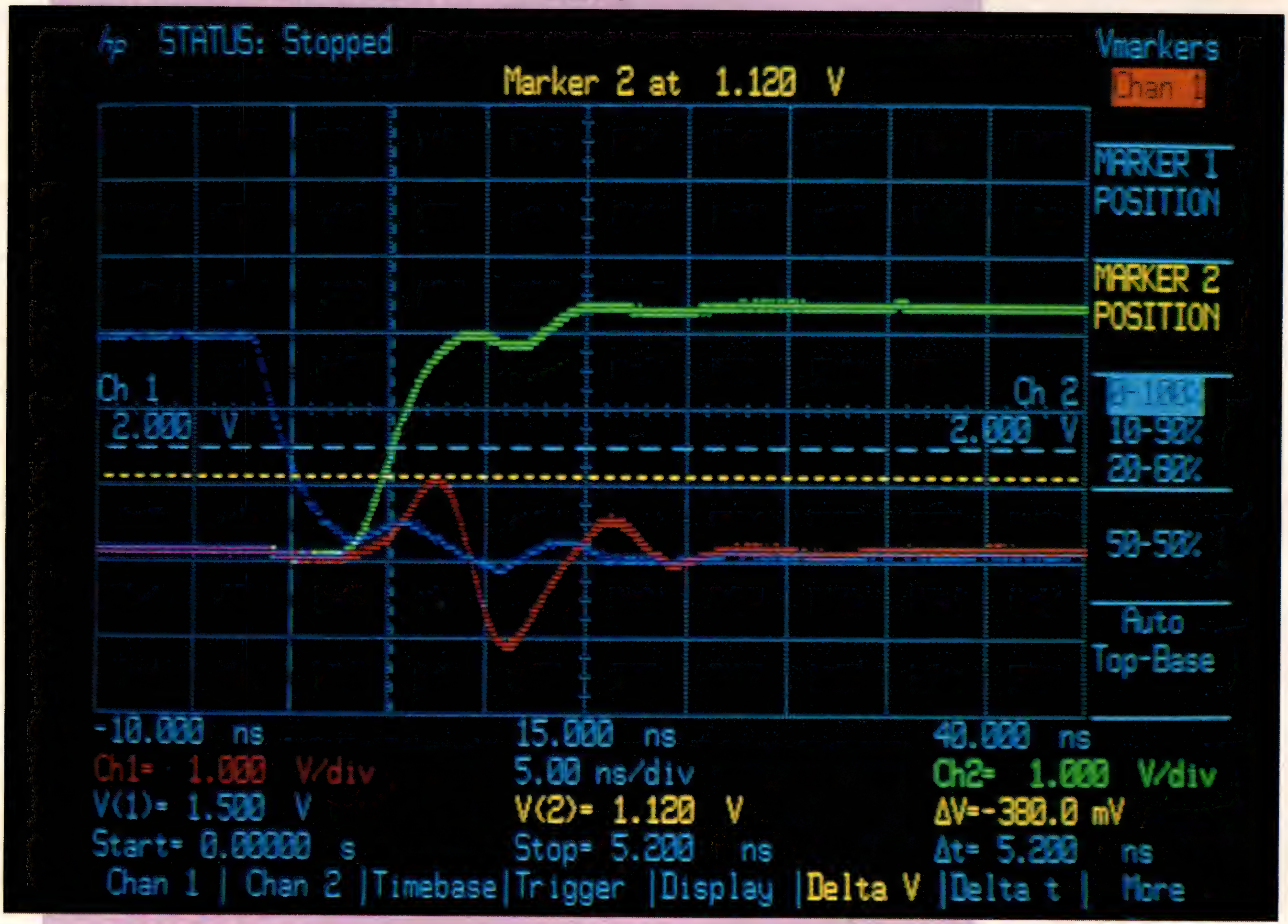
NATIONAL SEMICONDUCTOR 74F240PC



```
STATUS: Stopped
Marker 2 at 1.120 V
-10.000 ns              15.000 ns               40.000 ns
Ch1= 1.000 V/div        5.00 ns/div             Ch2= 1.000 V/div
V(1)= 1.500 V           V(2)= 1.120 V           ΔV=-380.0 mV
Start= 0.00000 s        Stop= 5.200 ns          Δt= 5.200 ns
```

DEVICE	D1	D2	D3	D4	D5
V_{OLP} (V) H-L	0.80	0.74	0.80	0.74	0.74
V_{OLP} (V) L-H	1.06	0.86	1.12	1.06	1.12
V_{OHV} (V) H-L	2.94	2.94	2.94	2.94	2.94
V_{OHV} (V) L-H	3.00	2.94	3.00	3.00	3.00
t_{PHL} (NSEC)	5.3	5.0	5.3	5.3	5.3
t_{PLH} (NSEC)	5.2	5.7	5.2	5.2	5.2
DATE CODE	8505	8505	8505	8505	8505

TEST CONDITIONS

V_{CC}=5.0V TEMP=22°C V_{IH}=3V V_{IL}=0V

UNSWITCHED OUTPUT PIN=18 SWITCHED OUTPUT PIN=16

DATA-SHEET SPECIFICATIONS

SUPPLY VOLTAGE=4.5 TO 5.5V OPERATING TEMPERATURE=0 TO 70°C
−55 TO +125°C (54)*

V_{IH}=2.0V V_{IL}=0.8V I_{OH}= −15 mA
−12 mA (54) I_{OL}=64 mA
48 mA (54)

POWER DISSIPATION (mW)

QUIESCENT	1 MHz	10 MHz
495	—	—

PROPAGATION DELAY (NSEC)

	TYP	0 TO 70°C	−40 TO +85°C	−55 TO +125°C (54)
t_{PHL}	3.5	—	6.0	5.7
t_{PLH}	5.1	—	9.0	8.0

NOTES:
THE SCOPE PHOTO AND THE HIGHLIGHTED COLUMN SHOW THE RESULTS FOR THE WORST-CASE DEVICE.
*SPECS LABELED "(54)" ARE FOR THE MILITARY-TEMPERATURE-RANGE VERSION OF THE SAME PART.

The Acid Test.

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Using an OMNI to program your PROMs, PALs and PLDs is *the way* to be sure that they will. It is known that programmable devices have higher failure rates than their non-programmable counterparts. To compound the problem, many devices contain logic that cannot be tested until *after* they are programmed.

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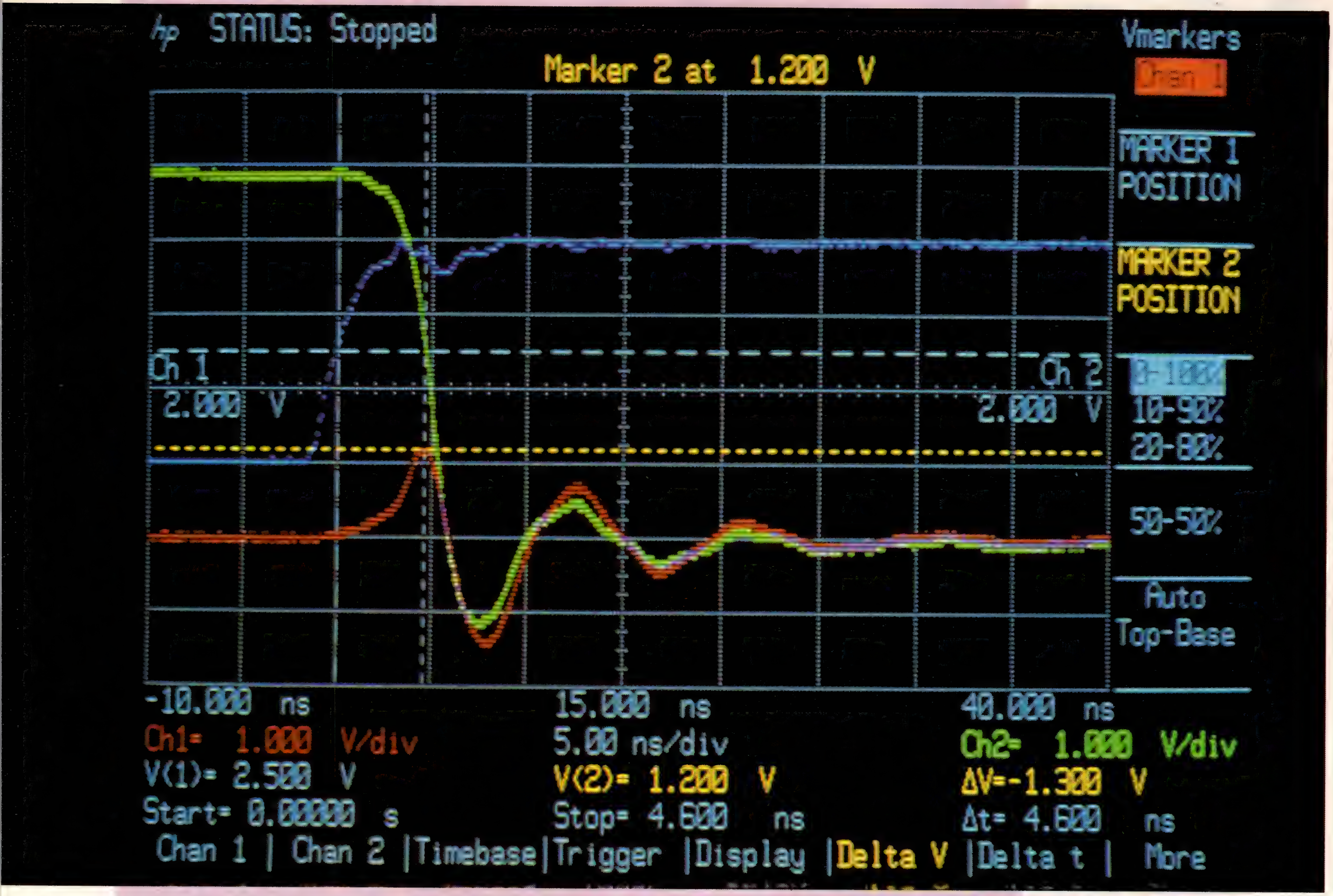
CIRCLE NO 57

SIGNETICS 74AC11240N



```
hp  STATUS: Stopped
                    Marker 2 at  1.200  V
Ch 1                                              Ch 2
 2.000  V                                     2.000  V
-10.000  ns          15.000  ns          40.000  ns
Ch1=  1.000  V/div   5.00 ns/div         Ch2=  1.000  V/div
V(1)= 2.500  V       V(2)= 1.200  V      ΔV=-1.300  V
Start= 0.00000  s    Stop= 4.600  ns     Δt= 4.600  ns
```

DEVICE	D1	D2	D3	D4	D5
V_{OLP} (V) H-L	1.06	1.18	1.12	1.18	1.20
V_{OLP} (V) L-H	0.30	0.20	0.30	0.24	0.30
V_{OHV} (V) H-L	4.38	4.38	4.38	4.38	4.38
V_{OHV} (V) L-H	3.94	4.00	3.88	3.94	3.94
t_{PHL} (NSEC)	4.7	4.6	4.6	4.5	4.6
t_{PLH} (NSEC)	7.1	5.2	5.3	5.3	6.4
DATE CODE	8833K	8833K	8833K	8833K	8833K

TEST CONDITIONS

V_{CC}=5.0V TEMP=22°C V_{IH}=4V V_{IL}=1V

UNSWITCHED OUTPUT PIN=2 SWITCHED OUTPUT PIN=10

DATA-SHEET SPECIFICATIONS

SUPPLY VOLTAGE=3.0 TO 5.5V OPERATING TEMPERATURE= −40 TO +85°C

V_{IH}=3.5V V_{IL}=1.5V I_{OH}=−24 mA I_{OL}=24 mA

POWER DISSIPATION (mW)

QUIESCENT	1 MHz	10 MHz
0.44	14	133

PROPAGATION DELAY (NSEC)

	TYP	0 TO 70°C	−40 TO +85°C	−55 TO +125°C
t_{PHL}	4.6	—	7.2	—
t_{PLH}	5.4	—	8.4	—

NOTES:
THE SCOPE PHOTO AND THE HIGHLIGHTED COLUMN SHOW THE RESULTS FOR THE WORST-CASE DEVICE.

"Thwap!"

When you're tired of hitting the wall–Signetics Programmable Logic Arrays offer those additional product terms you're aching for.

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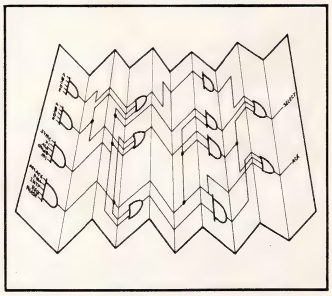

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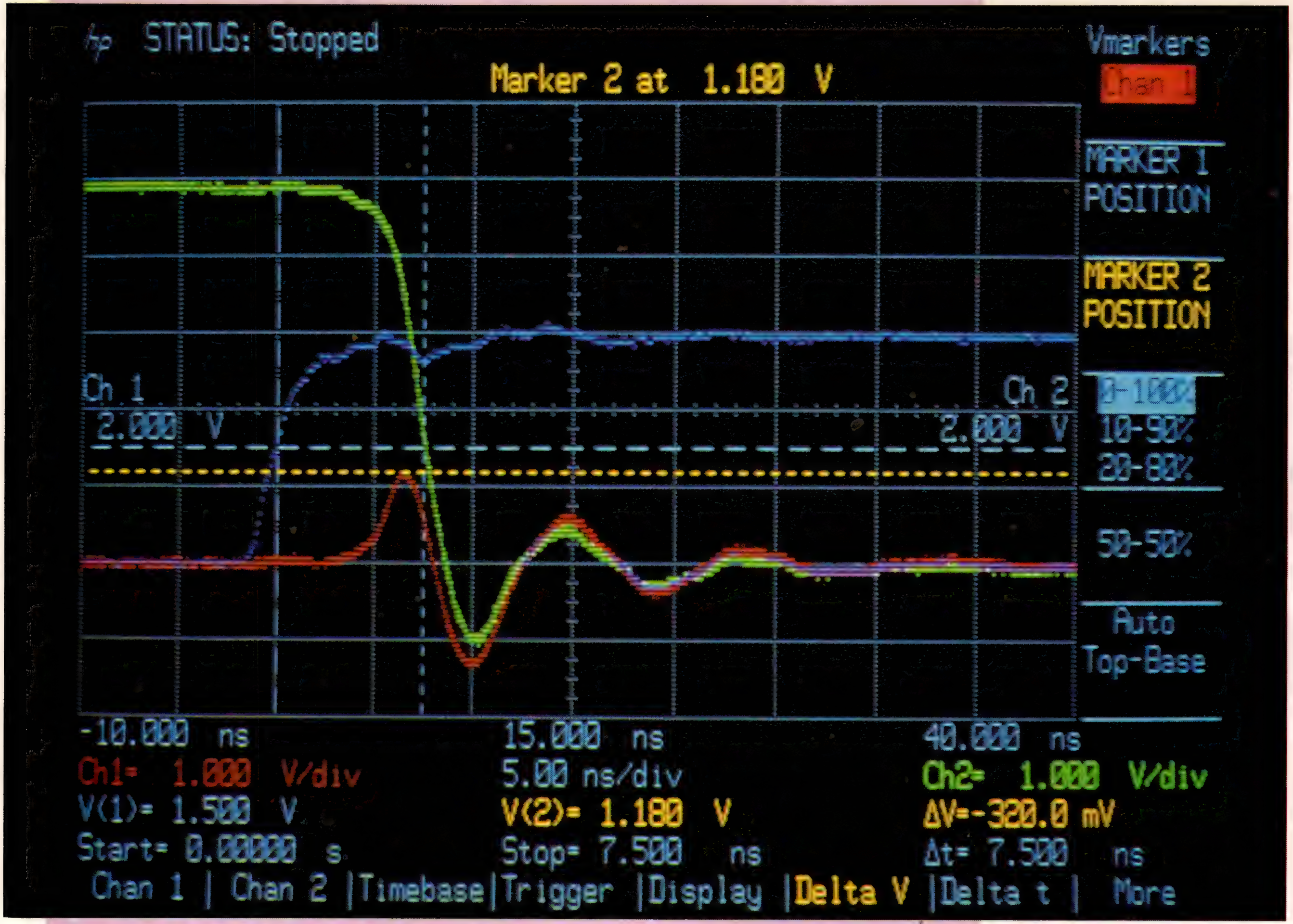


Marker 2 at 1.180 V

Ch1= 1.000 V/div
5.00 ns/div
Ch2= 1.000 V/div
V(1)= 1.500 V
V(2)= 1.180 V
ΔV=-320.0 mV
Start= 0.00000 s
Stop= 7.500 ns
Δt= 7.500 ns

DEVICE	D1	D2	D3	D4	D5
V_{OLP} (V) H-L	1.06	1.06	1.18	1.18	1.00
V_{OLP} (V) L-H	0.24	0.24	0.30	0.30	0.24
V_{OHV} (V) H-L	4.32	4.32	4.32	4.32	4.32
V_{OHV} (V) L-H	3.88	3.94	3.88	3.88	4.00
t_{PHL} (NSEC)	7.1	7.2	7.5	7.2	6.9
t_{PLH} (NSEC)	5.6	5.7	5.8	6.0	5.7
DATE CODE	8833K	8833K	8833K	8833K	8833K

TEST CONDITIONS

V_{CC}=5.0V TEMP=22°C V_{IH}=3V V_{IL}=0V

UNSWITCHED OUTPUT PIN=2 SWITCHED OUTPUT PIN=10

DATA-SHEET SPECIFICATIONS

SUPPLY VOLTAGE=4.5 TO 5.5V OPERATING TEMPERATURE= −40 TO +85°C

V_{IH}=2.0V V_{IL}=0.8V I_{OH}=−24 mA I_{OL}=24 mA

POWER DISSIPATION (mW)

QUIESCENT	1 MHz	10 MHz
0.44 TO 44	14 TO 36	136 TO 158

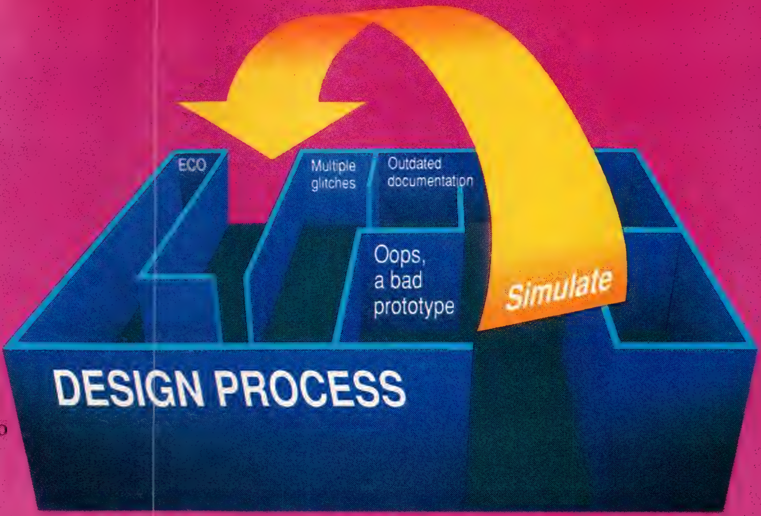
PROPAGATION DELAY (NSEC)

	TYP	0 TO 70°C	−40 TO +85°C	−55 TO +125°C
t_{PHL}	6.0	—	8.7	—
t_{PLH}	6.5	—	10.6	—

NOTES:
THE SCOPE PHOTO AND THE HIGHLIGHTED COLUMN SHOW THE RESULTS FOR THE WORST-CASE DEVICE.

OrCAD Answers Your Questions About

Logic Simulation



Q: Why simulate?

A: To save time.

The ideal development cycle is schematic to prototype to production. Simulation dramatically decreases the dreaded loop of schematic to prototype to schematic to prototype to schematic to...

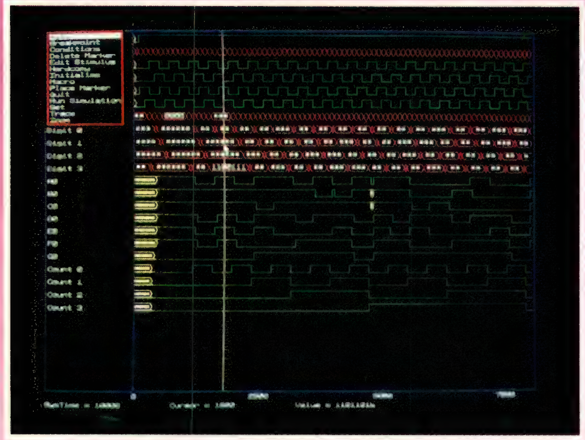
A: To save money.

If your design goes through several iterations, is the documentation still accurate? Suddenly your time and budget are being spent on laying in patches, not producing.

A: To make you look good.

Your schematic is supposed to be the best answer to someone else's design problem. Think of how great you'll look when you present a solution with no glitches, timing violations or other problems.

Verification of your design doesn't have to be handled at the prototype stage (or worse yet, the production stage).



R8839I

You need a digital simulator that helps you find timing violations and design anomalies before you spend time and money on prototypes. The result: fewer iterations, a shorter design cycle, a more reliable product and getting the project right.

Why OrCAD/VST?

A: OrCAD/VST enables you to interactively verify your design as it develops. A netlist from OrCAD's powerful Schematic Design Tools is all that's required to get started.

A: OrCAD/VST features a user interface similar to OrCAD/SDT III, including easy-to-use menu driven commands and powerful keyboard macros. Your valuable time is spent designing and testing rather than trying to learn a new system.

A: OrCAD/MOD extends OrCAD/VST to PLDs. A set of PLD Simulation Modeling Tools, OrCAD/MOD produces models of PLDs for OrCAD/VST to use in simulation of the larger circuit in which the PLD will operate.

A: OrCAD/VST offers unsurpassed performance on a PC. Independent benchmark tests have hailed OrCAD's logic simulator as superior to other simulators costing 20 times as much.

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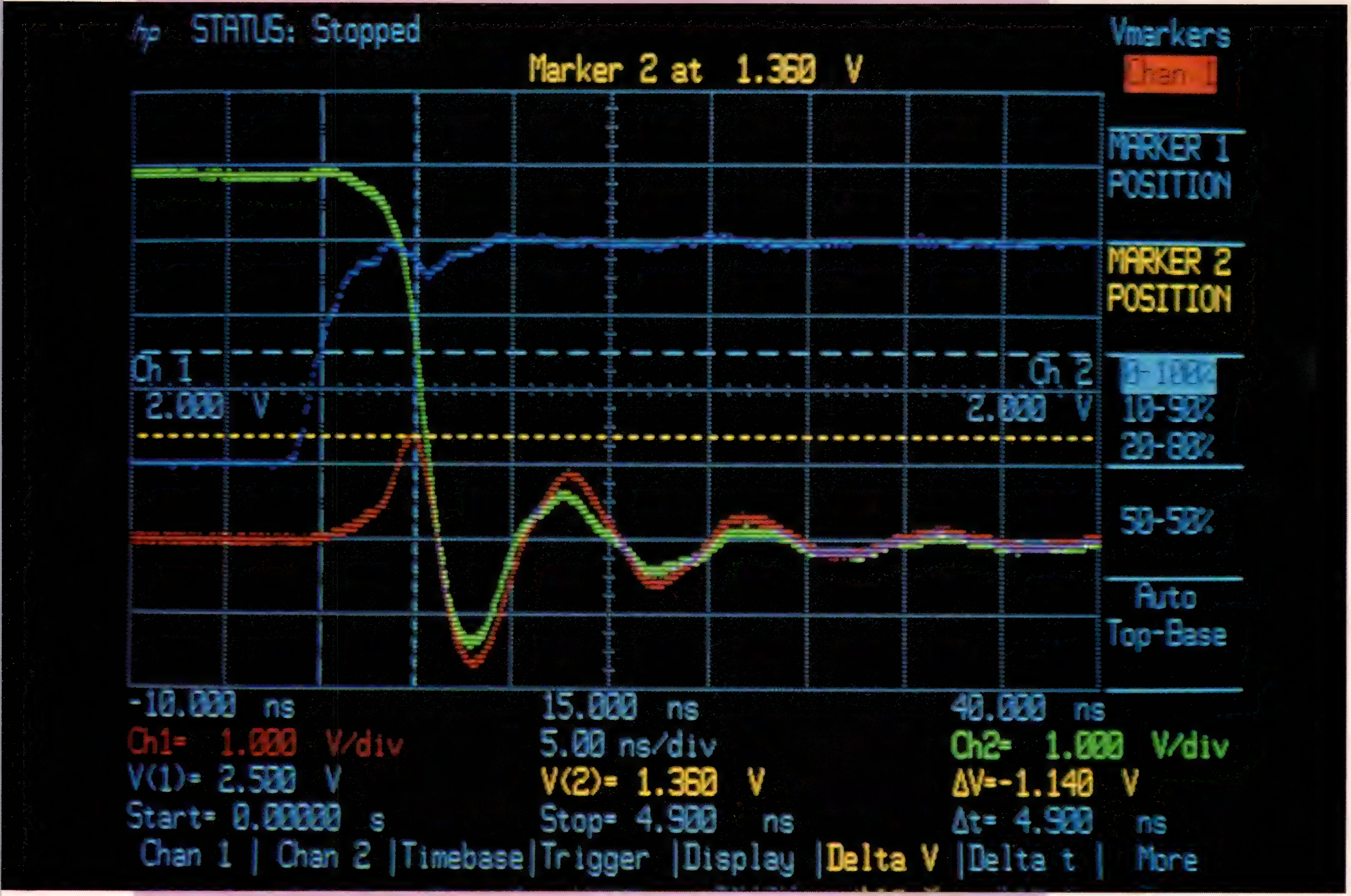
CIRCLE NO 59

TEXAS INSTRUMENTS 74AC11240NT



Marker 2 at 1.360 V

Ch1= 1.000 V/div   5.00 ns/div   Ch2= 1.000 V/div

V(1)= 2.500 V   V(2)= 1.360 V   ΔV=-1.140 V

Start= 0.00000 s   Stop= 4.900 ns   Δt= 4.900 ns

DEVICE	D1	D2	D3	D4	D5
V_{OLP} (V) H-L	1.30	1.30	1.30	1.36	1.36
V_{OLP} (V) L-H	0.24	0.24	0.24	0.24	0.24
V_{OHV} (V) H-L	4.32	4.32	4.32	4.32	4.32
V_{OHV} (V) L-H	3.94	3.94	4.00	3.94	3.88
t_{PHL} (NSEC)	4.6	4.6	4.7	4.9	4.7
t_{PLH} (NSEC)	5.5	5.5	5.6	5.6	5.5
DATE CODE	S8740AN	S8740AN	S8740AN	S8740AN	S8740AN

TEST CONDITIONS

V_{CC}=5.0V   TEMP=22°C V_{IH}=4V V_{IL}=1V

UNSWITCHED OUTPUT PIN=2   SWITCHED OUTPUT PIN=10

DATA-SHEET SPECIFICATIONS

SUPPLY VOLTAGE=3.0 TO 5.5V   OPERATING TEMPERATURE= −40 TO +85°C
−55 TO +125°C (54)*

V_{IH}=3.5V V_{IL}=1.5V I_{OH}=−24 mA I_{OL}=24 mA

POWER DISSIPATION (mW)

QUIESCENT	1 MHz	10 MHz
0.44	14	133

PROPAGATION DELAY (NSEC)

	TYP	0 TO 70°C	−40 TO +85°C	−55 TO +125°C (54)
t_{PHL}	4.6	—	7.2	7.8
t_{PLH}	5.4	—	8.4	9.0

NOTES:
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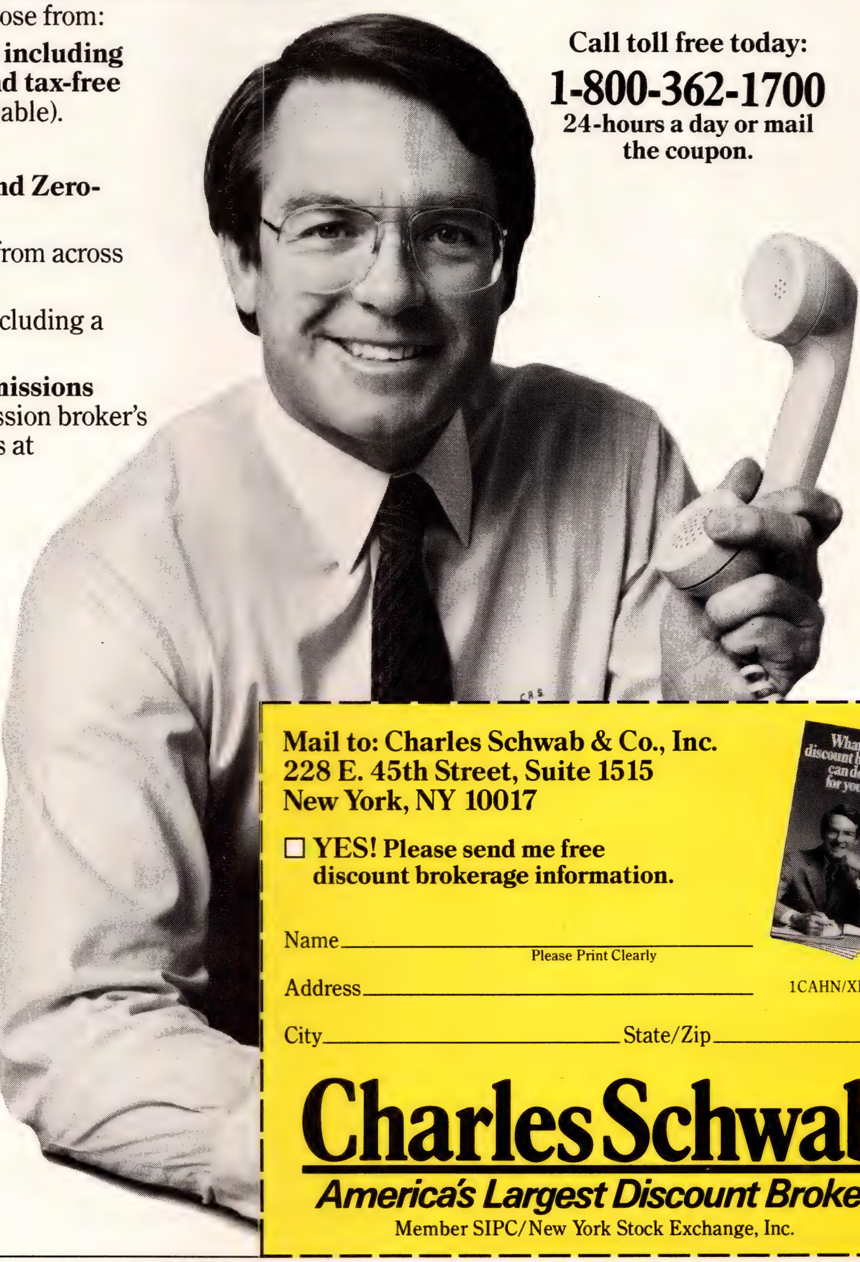

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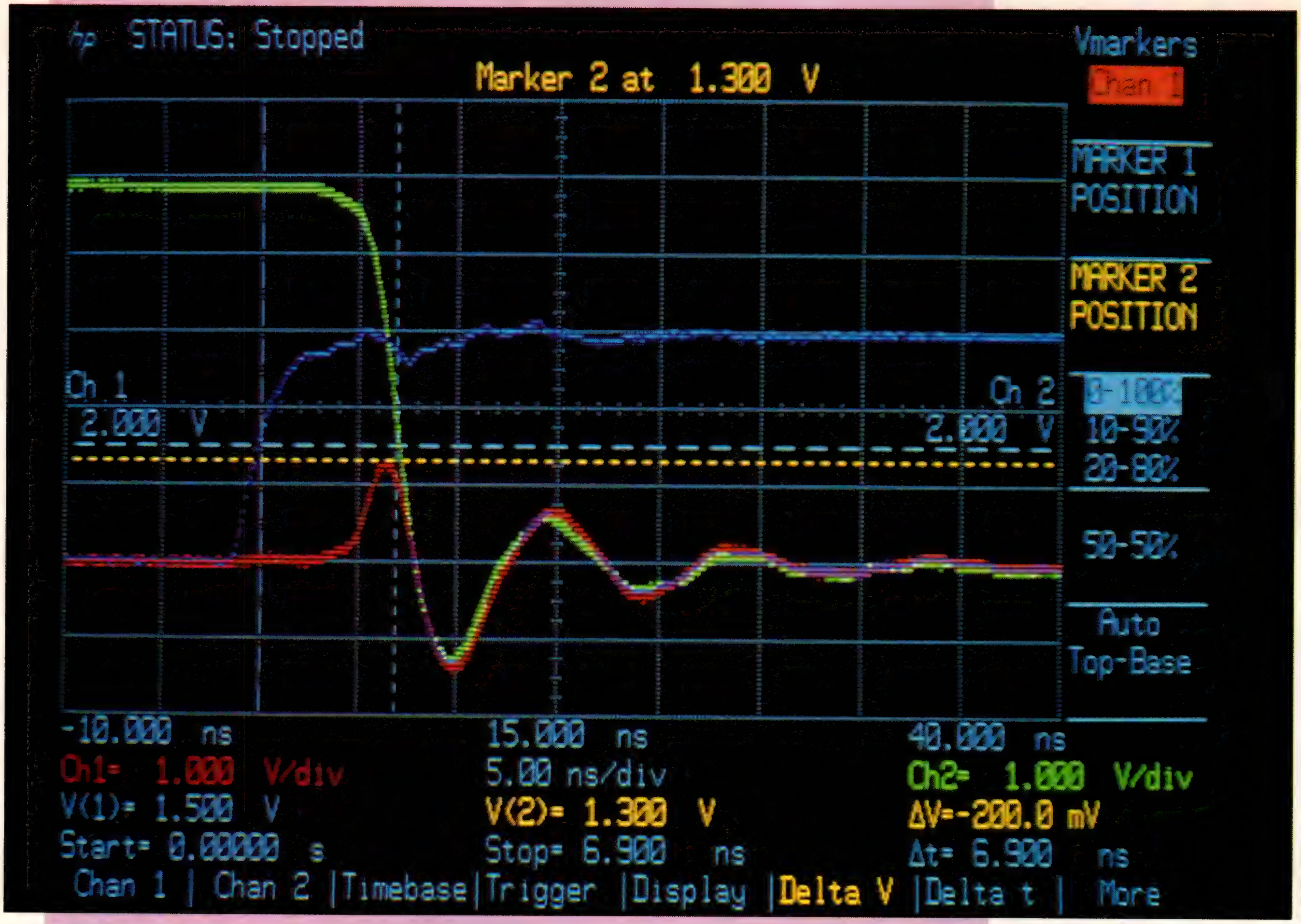

Marker 2 at 1.300 V

Ch1= 1.000 V/div
5.00 ns/div
Ch2= 1.000 V/div
V(1)= 1.500 V
V(2)= 1.300 V
ΔV=-200.0 mV
Start= 0.00000 s
Stop= 6.900 ns
Δt= 6.900 ns

DEVICE	D1	D2	D3	D4	D5
V_{OLP} (V) H-L	1.24	1.30	1.24	1.24	1.28
V_{OLP} (V) L-H	0.24	0.24	0.24	0.30	0.24
V_{OHV} (V) H-L	4.38	4.38	4.44	4.38	4.38
V_{OHV} (V) L-H	3.74	3.74	3.74	3.74	3.74
t_{PHL} (NSEC)	7.2	6.9	7.1	7.6	7.3
t_{PLH} (NSEC)	5.9	5.8	5.8	6.3	6.0
DATE CODE	S8723AN	S8723AN	S8723AN	S8723AN	S8723AN

TEST CONDITIONS

V_{CC}=5.0V TEMP=22°C V_{IH}=3V V_{IL}=0V

UNSWITCHED OUTPUT PIN=2 SWITCHED OUTPUT PIN=10

DATA-SHEET SPECIFICATIONS

SUPPLY VOLTAGE=4.5 TO 5.5V OPERATING TEMPERATURE= −40 TO +85°C
−55 TO +125°C (54)*

V_{IH}=2.0V V_{IL}=0.8V I_{OH}=−24 mA I_{OL}=24 mA

POWER DISSIPATION (mW)

QUIESCENT	1 MHz	10 MHz
0.44 TO 44	14 TO 36	136 TO 158

PROPAGATION DELAY (NSEC)

	TYP	0 TO 70°C	−40 TO +85°C	−55 TO +125°C (54)
t_{PHL}	6.0	—	8.7	9.2
t_{PLH}	6.5	—	10.6	11.1

NOTES:
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- One Octal Transparent Latch 3-State(Inverting)
- One Octal InvertingTransparent Latch 3-State

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CIRCLE NO 60

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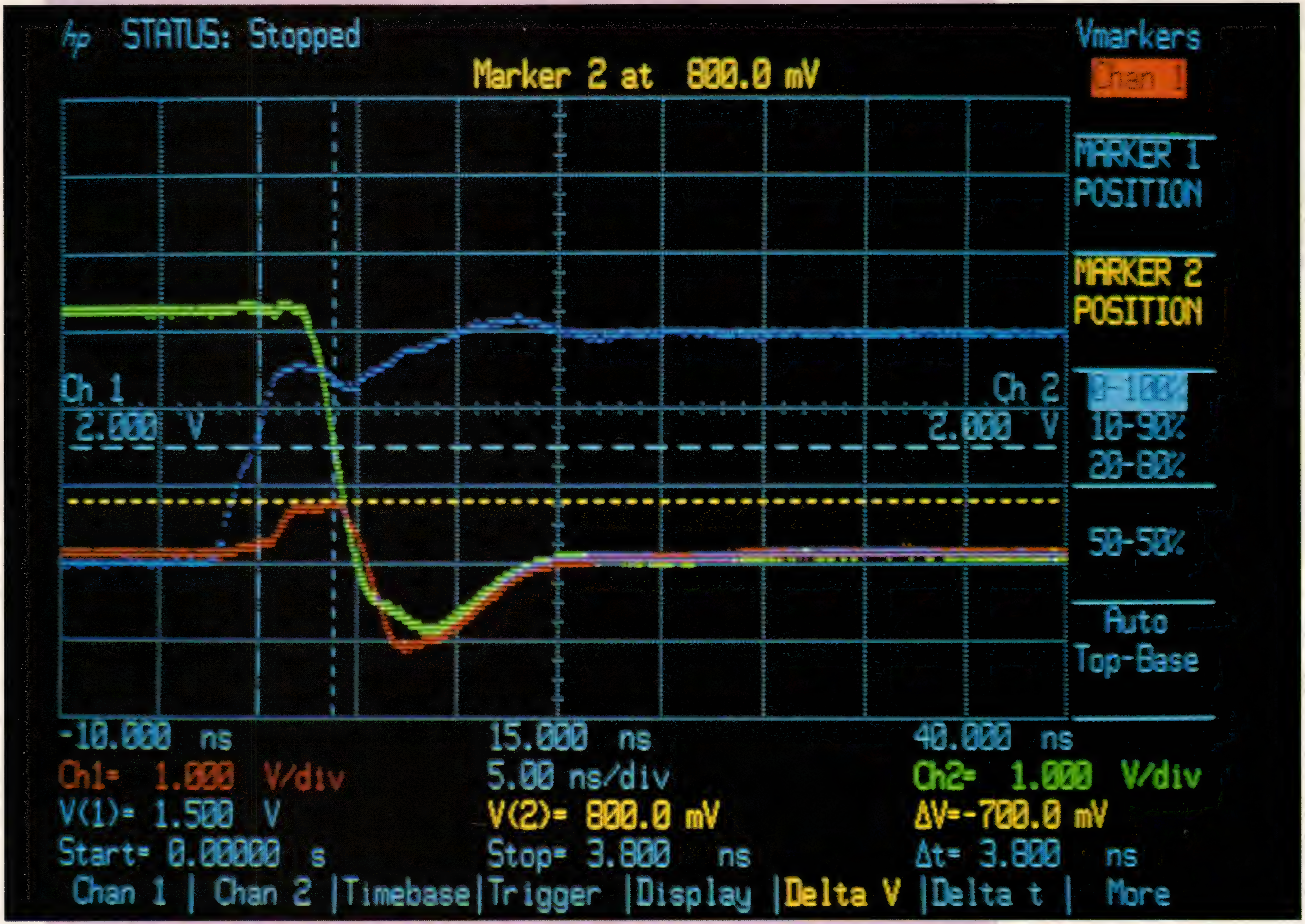
TEXAS INSTRUMENTS SN74BCT240N



STATUS: Stopped

Marker 2 at 800.0 mV

-10.000 ns
15.000 ns
40.000 ns

Ch1= 1.000 V/div
5.00 ns/div
Ch2= 1.000 V/div

V(1)= 1.500 V
V(2)= 800.0 mV
ΔV=-700.0 mV

Start= 0.00000 s
Stop= 3.800 ns
Δt= 3.800 ns

DEVICE	D1	D2	D3	D4	D5
V_{OLP} (V) H-L	0.80	0.80	0.80	0.80	0.80
V_{OLP} (V) L-H	0.44	0.44	0.44	0.44	0.44
V_{OHV} (V) H-L	2.88	2.88	2.88	2.88	2.82
V_{OHV} (V) L-H	3.00	2.94	3.00	2.94	2.94
t_{PHL} (NSEC)	3.8	3.9	3.9	3.9	3.8
t_{PLH} (NSEC)	4.4	4.3	4.3	4.3	4.3
DATE CODE	S8839BF	S8839BF	S8839BF	S8839BF	S8839BF

TEST CONDITIONS

V_{CC}=5.0V TEMP=22°C V_{IH}=3V V_{IL}=0V

UNSWITCHED OUTPUT PIN=18 SWITCHED OUTPUT PIN=16

DATA-SHEET SPECIFICATIONS

SUPPLY VOLTAGE=4.5 TO 5.5V OPERATING TEMPERATURE=0 TO 70°C
−55 TO +125°C (54)*

V_{IH}=2.0V V_{IL}=0.8V I_{OH}= −15 mA
−12 mA (54) I_{OL} = 64 mA
48 mA (54)

POWER DISSIPATION (mW)

QUIESCENT	1 MHz	10 MHz
391	—	—

PROPAGATION DELAY (NSEC)

	TYP	0 TO 70°C	−40 TO +85°C	−55 TO +125°C (54)
t_{PHL}	1.8	4.0	—	4.5
t_{PLH}	3.3	5.6	—	6.4

NOTES:
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CIRCLE NO 62

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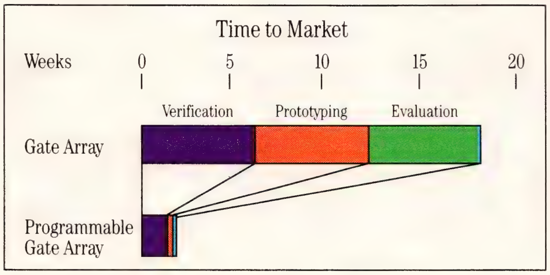

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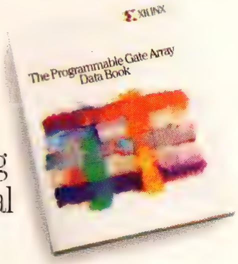

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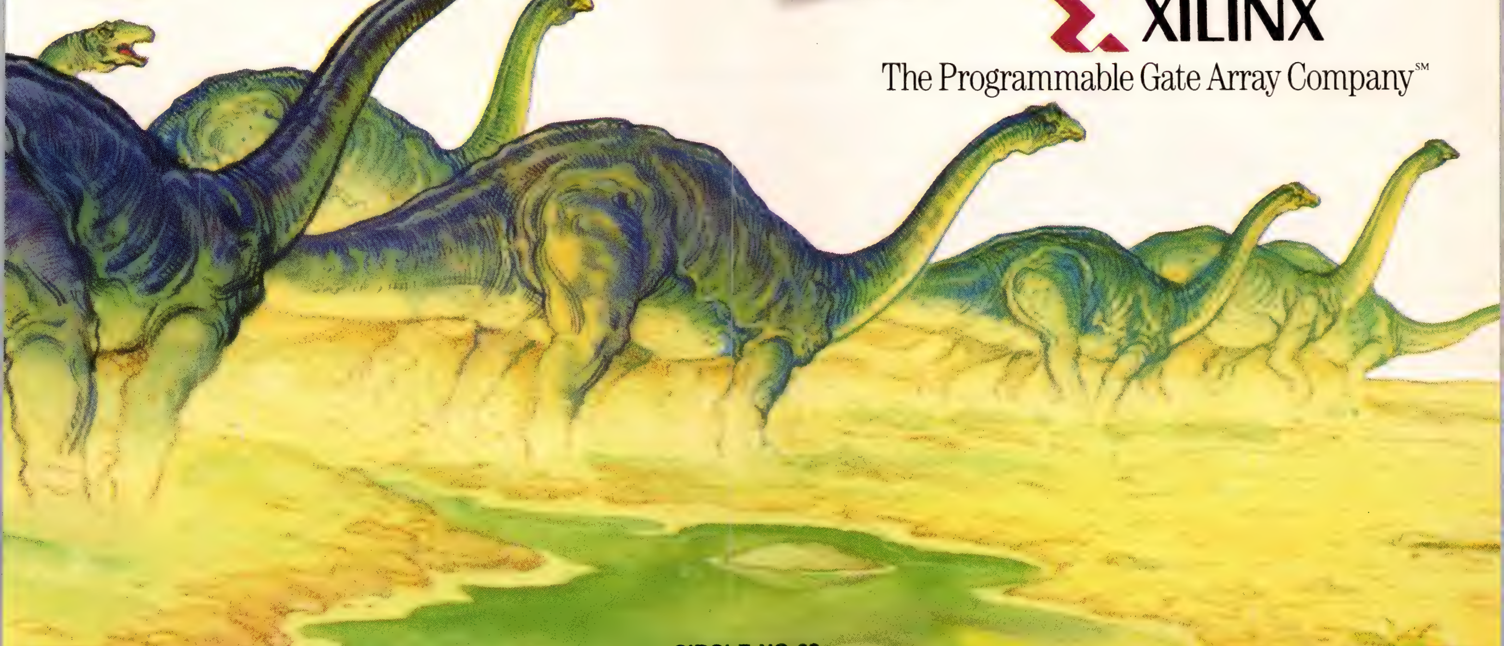
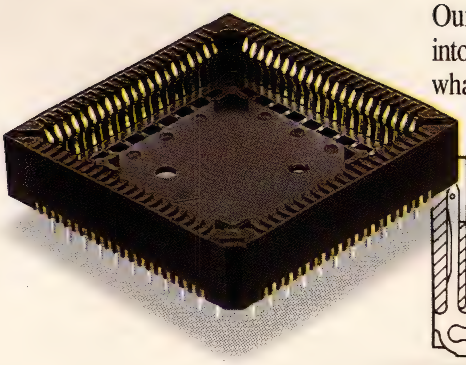


Any way you look at it—speed, density or price—Xilinx's Programmable Gate Arrays make conventional logic design seem prehistoric by comparison.

CIRCLE NO 63

A chip carrier socket that won't play "pop goes the circuit."



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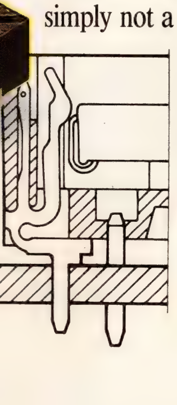
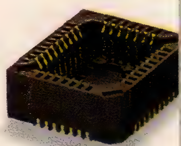


Controlled contact interface angle in AMP HPT sockets ensures positive chip carrier retention. Our exclusive removable housing allows direct inspection of solder joints, and fast repair/replacement of contacts.

The contacts are High Pressure Tin, an AMP proprietary design which creates very high normal forces—a minimum of 200 grams per contact—for maximum retention and reliable interconnection. Short-signal-path contacts float in the housing to accommodate thermal expansion.

Two basic styles of sockets are available: square or 32-position rectangular EPROM and SO-J. Both come in solder



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tail or surface mount versions and feature all the important details. Tin-over-nickel plating is applied after the contacts are formed, to assure full plating. We've built in visual indicators for locating pin 1, and polarizing to aid correct insertion.

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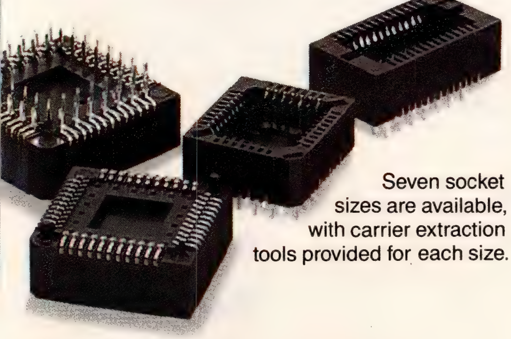
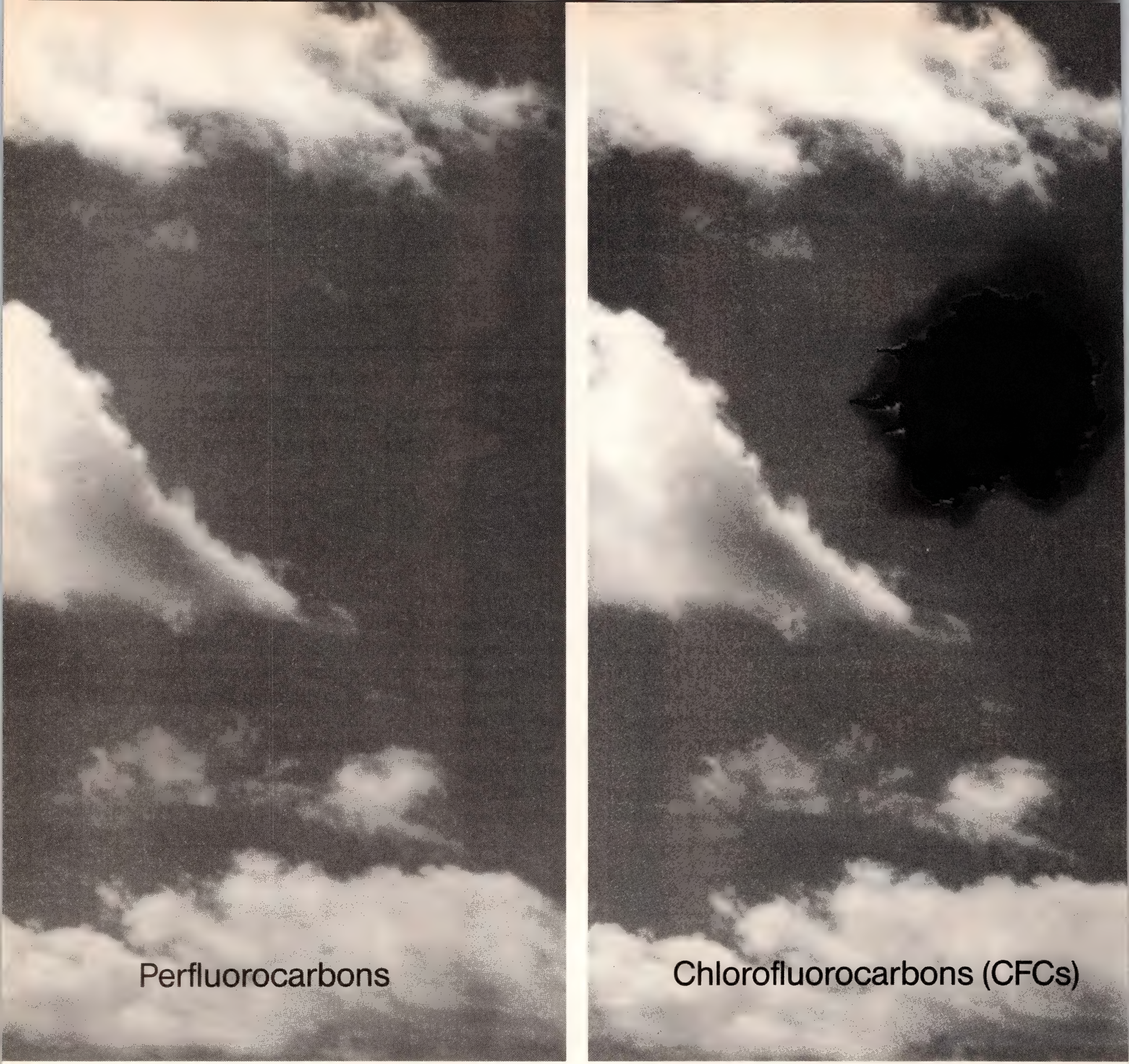
Call the AMP Information Center at 1-800-522-6752 for literature on HPT PLCC Sockets. AMP Incorporated, Harrisburg, PA 17105-3608.

AMP Interconnecting ideas



Seven socket sizes are available, with carrier extraction tools provided for each size.

CIRCLE NO 64



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3M

CIRCLE NO 65

Static column decode speeds up DRAM access time

Static column decode can't expedite µP throughput as well as cache memory can, but it is an inexpensive way to improve the performance of conventional 1M-bit dynamic-RAM (DRAM) chips.

Robert Breuninger, Loren Schiele, Joshua Peprah, *Texas Instruments Inc*

If you're designing a system based on a high-speed 32-bit µP like Motorola's 68020, you'll enjoy clock frequencies greater than 16 MHz and an addressing range of 4G bytes. But a fast clock speed and a large physical addressing range don't necessarily guarantee better performance. Memory access time, not processor speed, may be the deciding factor: If a processor must wait for data from its storage devices, its speed is clearly dependent on the memory bandwidth. And static column decoding can be a useful alternative to cache memory in some situations.

Cache memory is a popular solution for increasing the speed at which a processor receives data. A cache is a small, fast, static RAM (SRAM) that you can interpose between the processor and the slower dynamic RAM (DRAM) or main memory. In general, a cache memory offers high performance, but it's also expensive—not only do fast SRAMs cost more than DRAMs, but a cache also takes up additional board space. For these reasons, designers primarily use caches in computer systems that maintain large databases and need to maximize throughput.

Static column decode assumes same row address

A static-column-decode design offers a less expensive way to speed up access time. Static-column decode is a DRAM technique for obtaining high-speed read/write operations by reducing the number of cycles involved in signal setup, hold, and transition times. The name "static column decode" is misleading because what remains static in this technique is the row address; the column can change. ("Static" may refer to the fact that a DRAM that uses this technique acts like an SRAM.) After the first row access, $\overline{RAS}$ and $\overline{CAS}$ are both low, and the row address is latched in DRAM. Subsequently, for memory access in the same row, the timing diagram for a DRAM that uses static column decoding looks like a timing diagram for an SRAM. Although static-column-decode designs have limitations, they cost less than cache memories, and, in some circumstances, they perform almost as well.

If your primary design criterion is cost, the better solution may be static-column decoding. The method uses less hardware and lower-cost memory elements to enhance the performance of conventional DRAMs. And if in addition you use a cache in your design (and if your architecture is appropriate), you can also use static-column decoding to gain still higher levels of system performance.

Static column decoding is less expensive than designing in a cache memory.

During the first row access in static column decoding, the μP strobes a DRAM's row and column addresses in the normal manner by pulling the DRAM's $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ lines low. When both lines are held low, you can access new data simply by changing the column addresses; however, this technique assumes that the new address is in the same row as the current one. By accessing data in the same row, you can eliminate $\overline{\text{CAS}}$ precharging and strobing, and thus reduce access time. If, on the other hand, the new address is in a different row, you must perform a normal DRAM access cycle.

In order to use static column decoding, you obviously need a DRAM that permits this static-column-decode addressing. You also need a DRAM controller that can take advantage of static-column-decode addressing. Such a controller for the 68020, for example, is based on four key elements: a selectable refresh timer, a static-column-access detector, a DRAM control chip, and a programmable-sequence generator or timing controller (see **box,** "Designing a memory timer"). **Fig 1** shows an implementation of the static column decode for the 68020; it uses TMS4C1027s, which are 1M-bit devices that accommodate the static-column-decode addressing. The static-column-access detector performs the critical functions of determining whether the row location for the next address is the same or different from the previous one and indicating the results to the timing controller.

Technique avoids wait states

The timing diagram of **Fig 2** shows a normal DRAM read-access cycle. The cycle begins with the memory timing controller pulling both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ low and

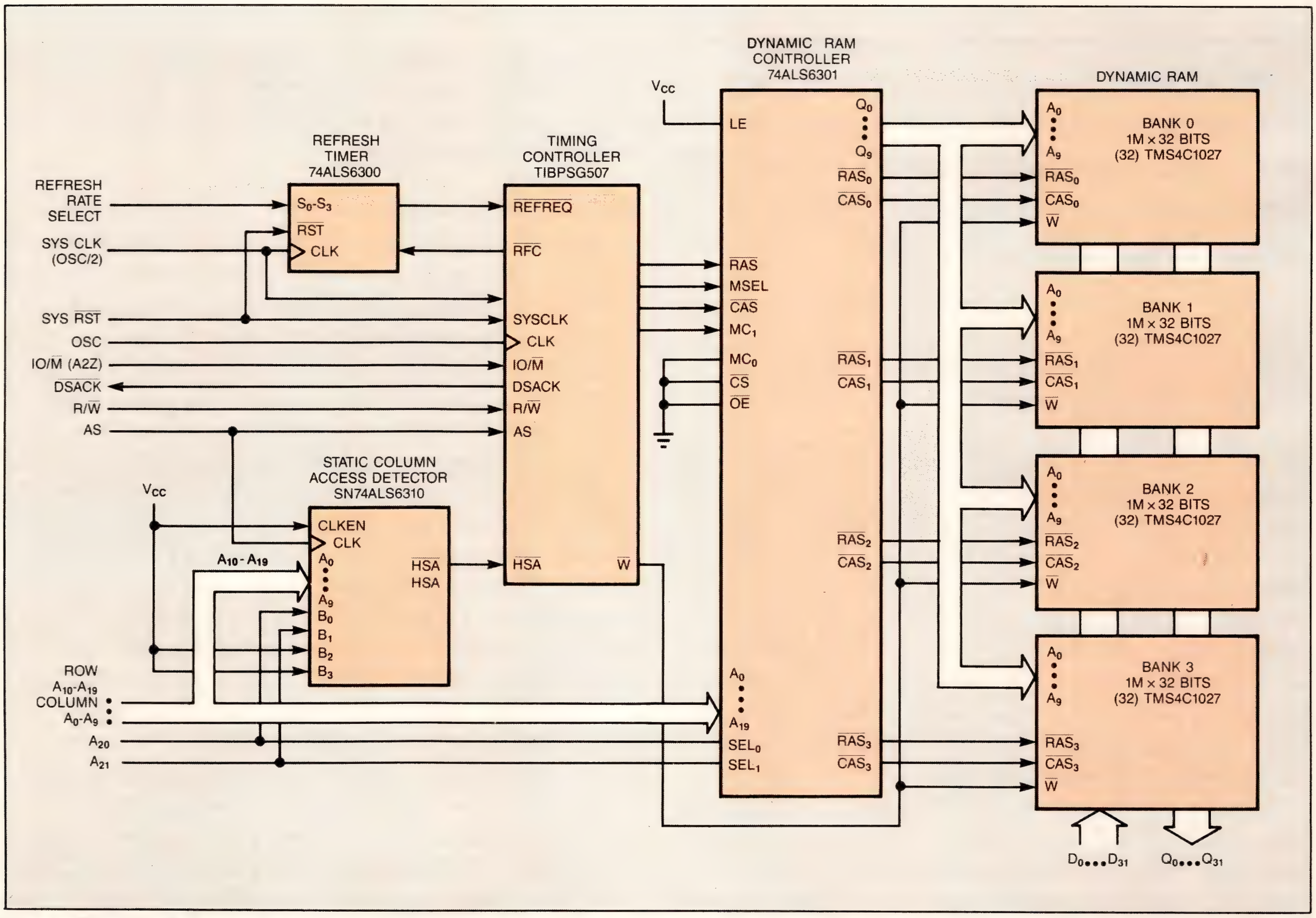

Fig 1—DRAMs that can use static column decoding *must be supported by a controller system, which provides the proper signals and timing. The 68020 controller shown here contains two unique devices for the task; a static-column access-detector chip and a timing controller implemented with a programmable logic device.*

presenting a valid address to the memory. In this configuration, a 68020 system requires a wait state of one clock cycle to guarantee that the read data is valid. If the system performs all access cycles in this manner, the processor faces a wait state during each read-access cycle, slowing overall access time and system throughput.

Assume that the next memory address is in the same row as the current one so that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ can stay low (just as they are at the end of the timing cycle in **Fig 2**). When both strobes are low, you avoid the wait state **(Fig 3).** When the static-column-access-detector signal ($\overline{\text{HSA}}$) is low, the timing controller knows that the next access will be from the same row as the last. The bank addresses must also remain unchanged; the access detector determines the state of these addresses.

In **Fig 3,** valid data appears at the memory output (Q_0 through Q_{31}) one oscillator-clock period after the column address of the complete memory address (MADR) becomes valid. TA_{CA} represents the time period between the valid column address and valid data on the memory output. (Note that TA_C is the read access time from $\overline{\text{CAS}}$ active.) In contrast to **Fig 2, Fig 3** requires no setup time for the column address. The result is that a memory controller can execute a high-speed access.

If you can design your system so that the majority of memory addresses are sequential (ie, in the same row), then most accesses will occur in static-column decode mode at speeds comparable to those available when using an SRAM or a cache memory.

When the system does need to switch rows, the cost in time is high: If $\overline{\text{HSA}}$ is high, it indicates that the static-column-access detector knows that the next access is from a different row than the current one. In this extended access cycle, the system must bring $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to a high level in order to strobe in the new row and column addresses. Moreover, the system must meet the precharge-time requirement of the DRAM before $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ can go low again. As a result, when the system changes rows, it takes three clock cycles or wait states to access memory.

If your system can't operate for the most part sequentially, then it's faster to execute normal access cycles rather than to go through a high-speed access followed by an extended access. You can still take advantage of static column decode, however, by using the high-speed access mode only when the system moves blocks of data, as it does in DMA operations.

Detector determines next access

The static-column-access detector performs the basic operation of determining whether the next access is from the same row of the DRAM as the current access **(Fig 4).** In a 68020-based microprocessor system like the one in **Fig 1**, the processor's A_{10} through A_{19} address bits connect to the 10 most significant bits of the row portion of the detector's present-address register (A_0 through A_9). Two of the inputs for the bank portion

Designing a memory timer

Of the four chips in this system, the timing controller is most subject to variation because it generates the timing sequences for your memory devices. Therefore, instead of designing a large family of devices to handle a host of contingencies, you can implement the timing-controller circuit using programmable logic, which lets you customize the timing sequences for your system.

Two software packages can each generate the fuse map necessary to program logic devices and so simplify timer design. CUPL is offered by Logical Devices Inc (Fort Lauderdale, FL, (800) 331-7766). The other package, ABEL, is a product of FutureNet, a Division of Data I/O Corp (Redmond, WA, (800) 247-5700).

CUPL and ABEL reduce the number of equations you need to generate a timing function and generate the actual fuse map for blowing the internal fuses of a programmable device. Both packages are also efficient. For example, it takes just 54% of a TIBPSG507 programmable sequence generator's product terms—43 of its 80 terms—to implement a timing controller for static column decode. This efficiency gives you a substantial margin for modifying or adding to timing sequences to meet specific system requirements.

By holding the row and address strobes low, you can avoid wait states between memory accesses.

of the present-address register come from the 68020's A_{20} and A_{21}, respectively. (This example uses only 4 of a possible 16 banks.) The 68020's address-strobe (AS) signal connects to the clock (CLK) line of the 6310.

When the processor pulls AS low, row and bank data move from the present-address register to the corresponding portions of the previous-address register. Simultaneously, new row and bank data go into the present-address register. A comparator circuit looks at both sets of data to determine whether they are equal.

If they are equal (that is, the next access is in the same row as the latest one), the comparator generates a low signal on the $\overline{\text{HSA}}$ line. If the data sets are unequal, $\overline{\text{HSA}}$ goes high and an extended access cycle occurs.

$\overline{\text{HSA}}$ connects to a timing-control IC that generates memory timing signals (such as $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and MSEL). A dedicated refresh timer IC then generates the refresh timing signals for the DRAMs. The specifications of the DRAM determine the refresh timing intervals; industry-standard specs require that you refresh 1M-bit DRAMs once every 8 msec.

DRAM architecture defines refreshing

Because of the way a DRAM is partitioned internally, you need to access only half the number of rows in order to refresh the memory (eg, 512 rows for a 1M-bit × 1 device). In effect, this architecture means that your system must refresh each row at least once every 15.6 μsec—8 msec to refresh 512 rows. If your 68020-based system operates at a clock rate of 10 MHz, for example, the refresh timer would generate a refresh request ($\overline{\text{REFREQ}}$) at least every 15.6 μsec, or once every 156 timing cycles.

The timing controller receives the refresh request

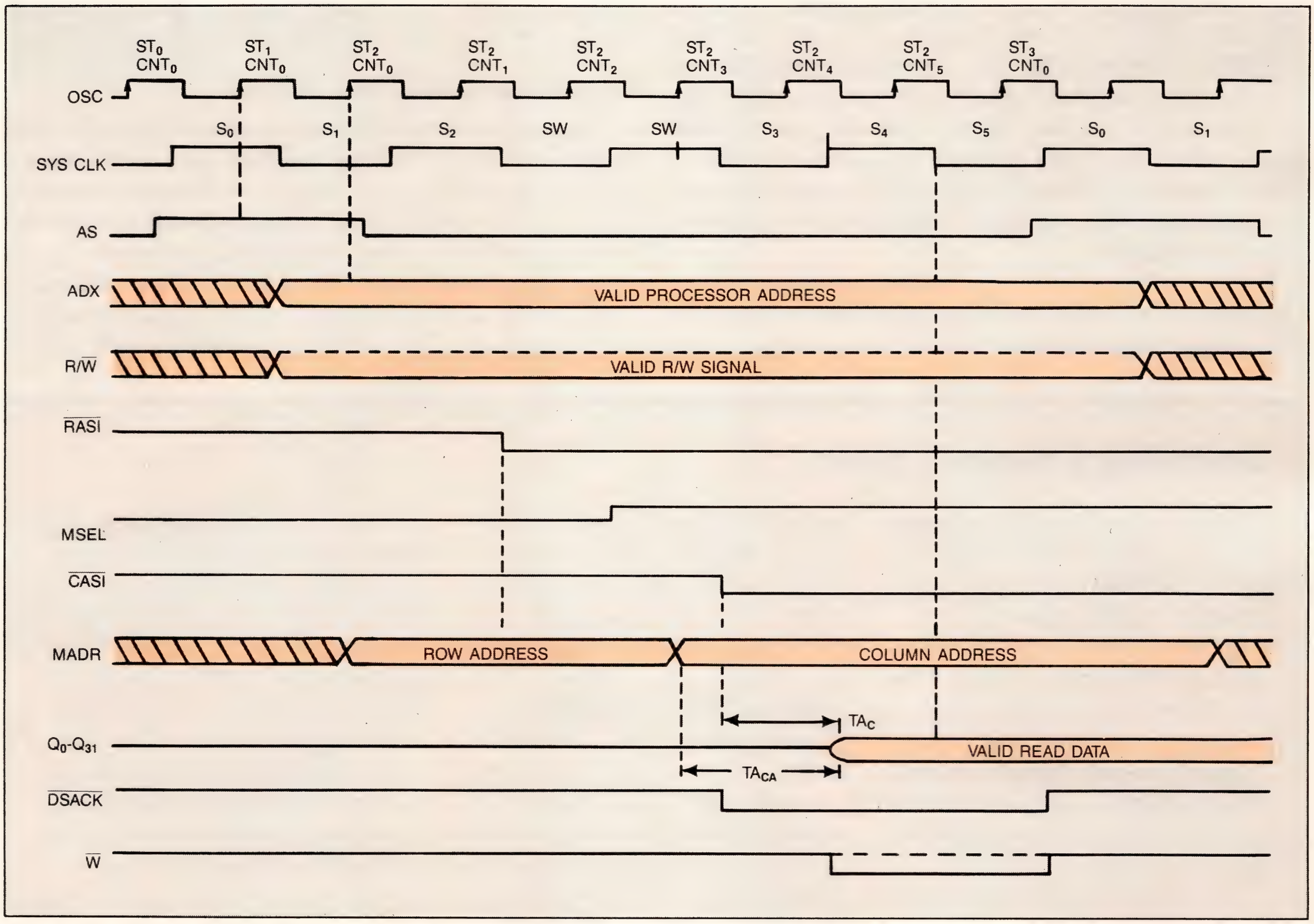

Fig 2—In a normal access cycle, *the memory timing controller addresses a DRAM by pulling both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ low after presenting a valid address. But each normal cycle requires a one-cycle wait state, increasing access time to the DRAM and reducing system throughput.*

and returns an $\overline{RFC}$ signal to the refresh timer when the refreshing is completed. You must hardwire the ALS6300's input select lines (S_0 through S_3) to match the 68020 μP's clock frequency, which, in turn, selects the correct refresh rate. In refresh mode, two internal 10-bit counters cycle through the refresh addresses. You can design your timing controller to use a distributive or burst refresh.

The timing controller is very important because DRAM operations depend primarily on how the memory is timed. The timing chip generates all of the timing sequences for the system.

The system in **Fig 1** has nine possible sequences or states (STs). The flow chart in **Fig 5** illustrates these states by the designations ST_0 through ST_8. Four of these states, ST_0, ST_1, ST_3, and ST_4, are holding and transition states that lead into the various timing sequences. Of the five remaining states, ST_2 is normal access, ST_5 is extended access, ST_6 is high-speed access, ST_7 is normal refresh, and ST_8 is extended refresh. The flow chart matches the timing diagrams of **Figs 2 and 3.** Note that the oscillator cycles in the timing diagrams are labeled with ST numbers to illustrate the switching activity on the key signal lines

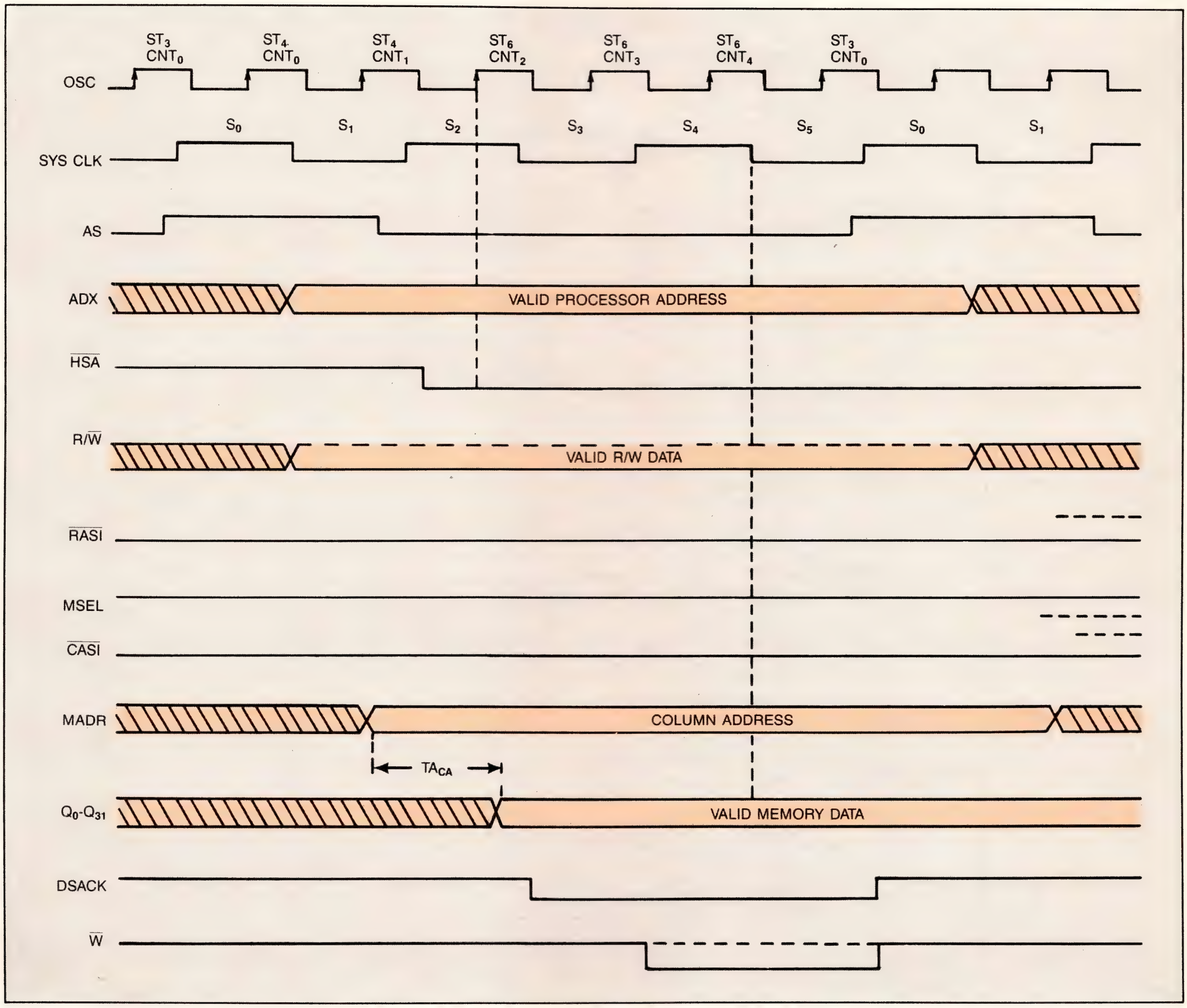

***Fig 3—Static-column decode permits a DRAM** to obtain data through a high-speed access cycle that eliminates the wait states of the normal cycle in **Fig 2**. Note that no $\overline{RAS}$ and $\overline{CAS}$ switching is required; the signals remain in the low state from the previous access cycle.*

during various states.

In **Fig 1,** the 74ALS6301 DRAM controller is the heart of the memory system. This controller can control DRAMs that have a 1M-bit capacity. Although the DRAM controller can operate in any of four modes (selected by logic levels applied to its MC_0 and MC_1 lines by the timing controller), for the design in **Fig 1,** MC_0 is grounded, making just two modes possible: refresh without scrubbing and read/write.

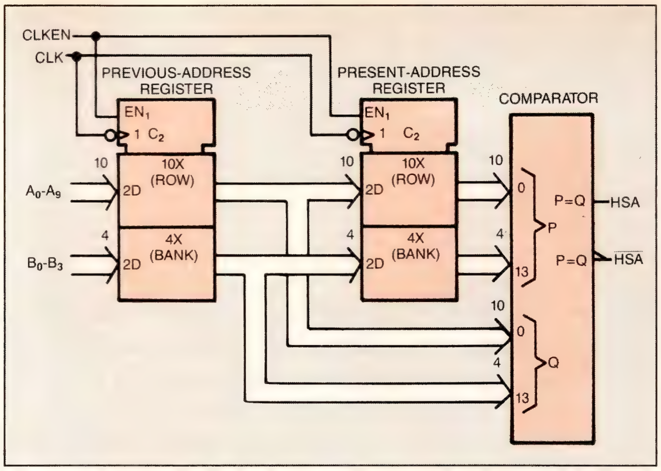

***Fig 4—A static-column access detector** determines whether the next access cycle is from the same row of the DRAM as the last access. Two registers compare addresses and send a control signal to the timing circuit indicating the same, or a different row.*

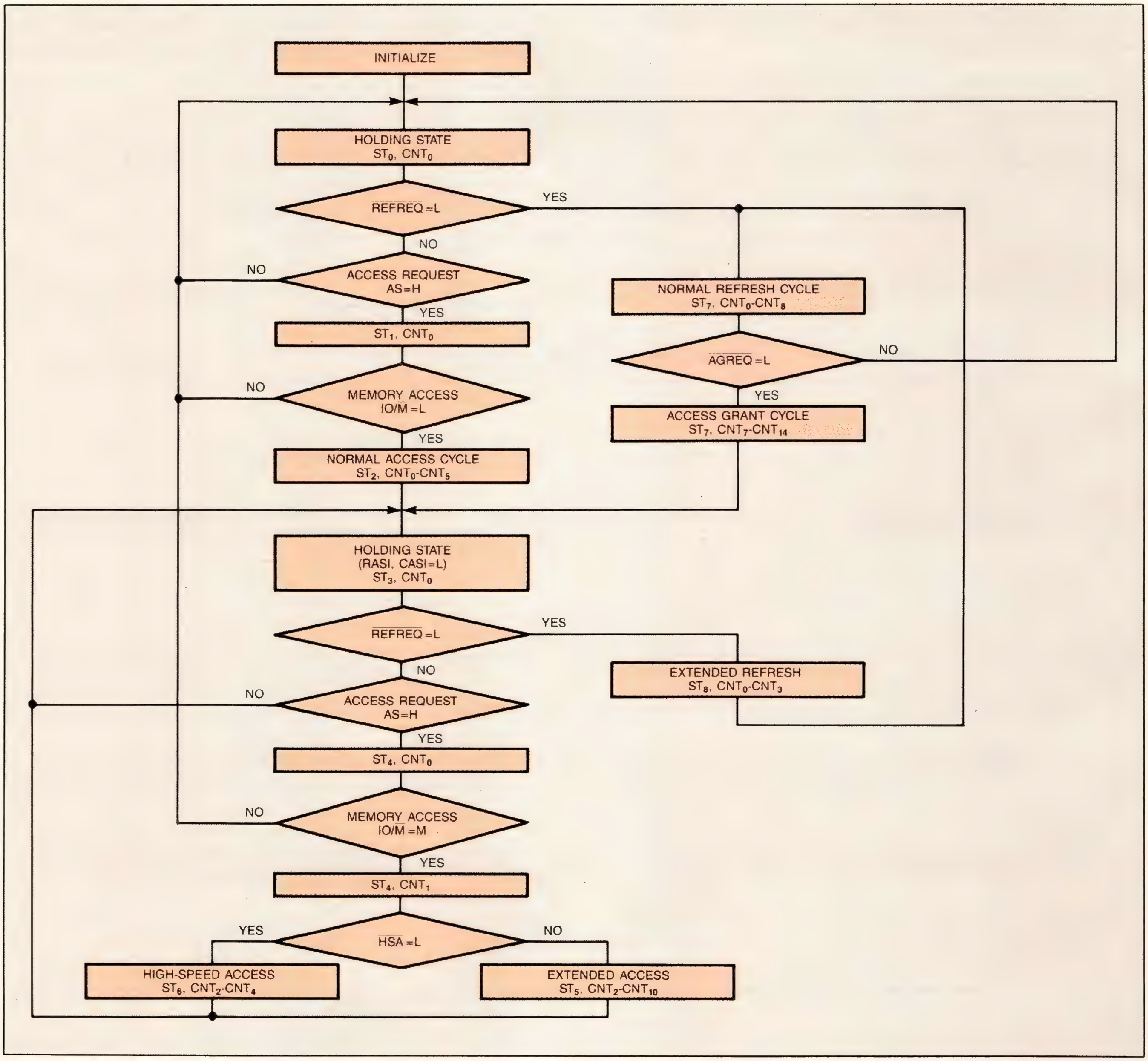
INITIALIZE
HOLDING STATE ST_0, CNT_0
$\overline{REFREQ}$ =L
YES
NO
ACCESS REQUEST AS=H
NO
YES
ST_1, CNT_0
MEMORY ACCESS IO/$\overline{M}$ =L
NO
YES
NORMAL ACCESS CYCLE ST_2, CNT_0-CNT_5
NORMAL REFRESH CYCLE ST_7, CNT_0-CNT_8
$\overline{AGREQ}$ =L
NO
YES
ACCESS GRANT CYCLE ST_7, CNT_7-CNT_{14}
HOLDING STATE (RASI, CASI=L) ST_3, CNT_0
$\overline{REFREQ}$ =L
YES
NO
EXTENDED REFRESH ST_8, CNT_0-CNT_3
ACCESS REQUEST AS=H
NO
YES
ST_4, CNT_0
MEMORY ACCESS IO/$\overline{M}$ =M
NO
YES
ST_4, CNT_1
$\overline{HSA}$ =L
YES
NO
HIGH-SPEED ACCESS ST_6, CNT_2-CNT_4
EXTENDED ACCESS ST_5, CNT_2-CNT_{10}

***Fig 5—This flow chart illustrates** the entire timing sequence of the timing controller implemented in a TIBPSG507 programmable sequence generator. The nine timing states (ST_0 thorough ST_8) can handle any type of DRAM access cycle—normal, high-speed, or extended.*

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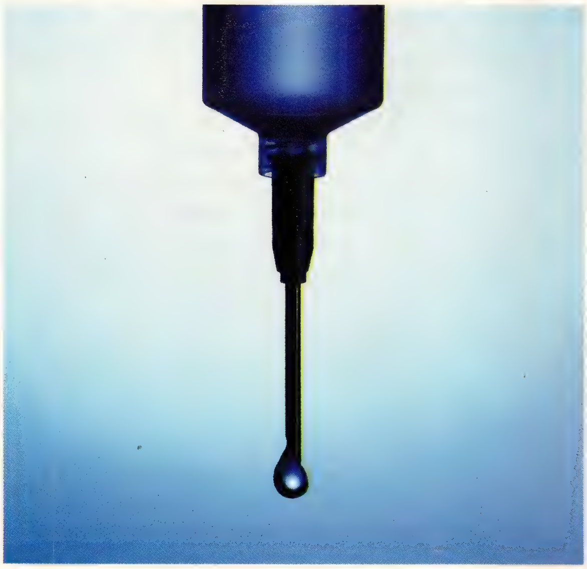

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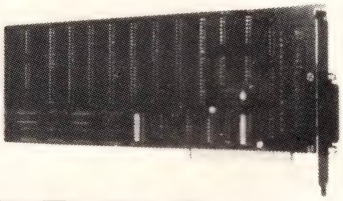

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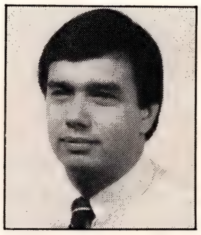
In the first mode, refresh without scrubbing, the timing controller performs refresh cycles using only the row counter to generate addresses. All four $\overline{\text{RAS}}$ outputs are active, while the four $\overline{\text{CAS}}$ outputs remain high. A scrubbing operation would implement and execute an error-correction cycle during a refresh cycle. For scrubbing, you would use an error-detection and -correction chip like the 74AS632.

During read/write mode, the DRAM controller multiplexes row- and column-addresses to the DRAMs, and the timing controller activates the corresponding $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals to strobe the addresses into memory. It uses the MSEL line to select the addresses. A high MSEL signal selects the column address, and a low one selects the row address.

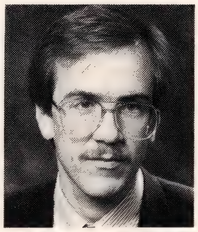
A single ALS6301 can control 4 banks of memory. But you can control more banks by using additional controllers together with simple logic to decode a chip-select ($\overline{\text{CS}}$) input for each controller. EDN

Authors' biographies

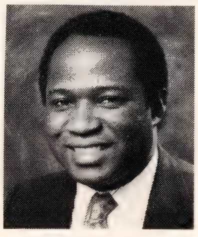
Robert Breuninger is a VLSI applications engineering manager for Texas Instruments (Dallas, TX), where he has worked for 10 years. He earned his BS in electrical and computer engineering at Oregon State University. In his spare time, Robert enjoys golfing and fly fishing.



Loren Schiele is an applications section manager for TI responsible for cache-memory support and new-product evaluation. He has worked for Texas Instruments for eight years. Loren holds a BS degree in electrical engineering from Montana State University. He spends his spare time with this wife and 2-year-old son.



Joshua Peprah is a VLSI application engineer in programmable devices and cache-tag memory products. He has been with Texas Instruments for five years. Joshua graduated from the Royal College of Science in England with a BSEE and from Texas Christian University with an MBA. He likes outdoor sports and classical literature.



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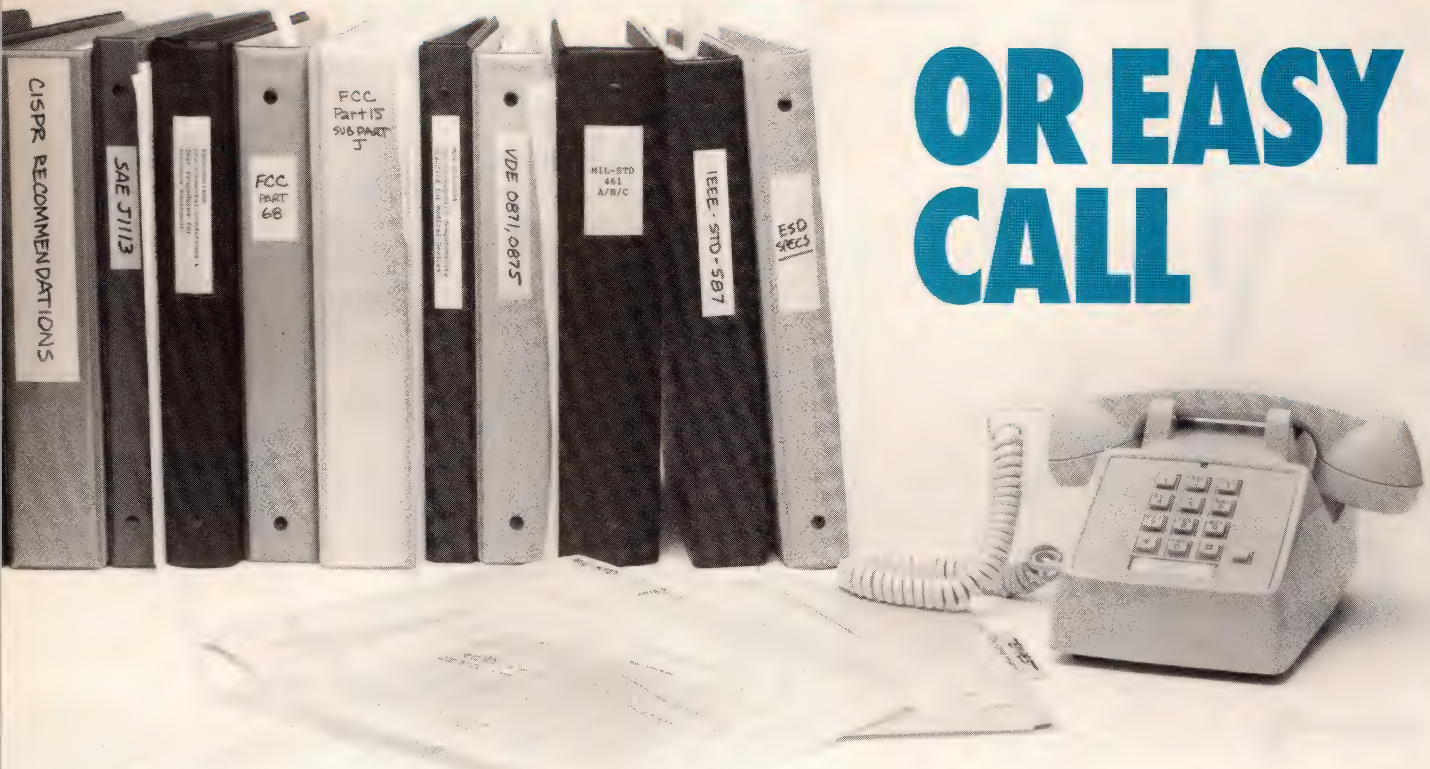

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A state machine handles back-end processing for clustered networks

Often, systems designers focus on the front-end protocols in network communications. But when a data network interfaces with many multiplexed devices through a gateway, the heavy back-end traffic can cripple a μP. A state machine can assume most of these back-end communication tasks.

Brian Bennett, *McDonnell Douglas Electronic Systems Co*

When a packet-switching integrated digital network (IDN), such as one conforming with CCITT Recommendation X.25, interfaces with a time-division-multiplexed (TDM) IDN, such as a private branch exchange (PBX), a gateway translates the communication protocols **(Fig 1)**. A variety of VLSI chips can offload the front-end X.25 Level 2 tasks from a controlling μP. However, when a PBX interconnects a cluster of 100 or more terminals, the back-end communication tasks can quickly overwhelm the μP. A gateway based on a state-machine design alleviates this problem. The state machine relieves the μP of transferring characters to and from the terminals at their appropriate baud rates.

A block diagram for a gateway module that interfaces a data network using X.25 protocols and a PBX's TDM bus is shown in **Fig 2.** Commercially available protocol controller chips, such as AT&T's T7102, Western Digital's WD255-01, and Motorola's MC68605, can easily handle the Level 2 tasks of X.25. The gateway must also conform to Level 3 of X.25 and the Packet Assembler Disassembler (PAD) requirements specified by CCITT Recommendation X.3 (see **box,** "The CCITT recommends specific PAD standards"). A state-machine implementation of the PAD functions eliminates potential bottlenecks caused by heavy traffic.

The PAD must process data in two directions. In one direction, the PAD must process data that arrives over the X.25 link before relaying it to a terminal on the PBX cluster. For example, the PAD must first determine if there are any special services required before relaying the data. Special services may include

- discarding the output (parameter 8)
- adding padding characters after a carriage return (CR) (parameter 9)
- line folding (parameter 10)
- inserting a CR after a line feed (LF) (parameter 13)
- adding padding characters after an LF (parameter 14)
- providing the page wait feature. (parameter 22)

The PAD must assemble a transmit buffer to perform these special services. The transmit buffer is a portion of the gateway's main memory that is shared by the PAD and the controller IC. The PAD must transfer the data in the transmit buffer to the appropriate port on the TDM bus at a baud rate suitable for each port.

When transferring data in the other direction, that

A state-machine implementation of the PAD functions eliminates potential bottlenecks caused by heavy traffic.

is, from the terminals on the PBX to the X.25 network, a primary concern is data overflow in the input FIFO buffer, which is located in the bus interface. Because the input FIFO buffer has limited storage space, the PAD must remove the incoming characters from the FIFO buffer and place them in an edit buffer for processing before passing it on to the controller IC. This edit buffer is located in the gateway's shared memory.

The PAD is also responsible for maintaining control of the data flow to and from the terminals. The XON and XOFF control characters control communications with a start-stop terminal. The μP must issue an XOFF character to this terminal if the PAD is unable to allocate new buffers for incoming data from the terminal. This situation can occur if the X.25 link is oversubscribed or if the gateway has insufficient shared memory space.

Similarly, the terminal issues XON and XOFF control characters to the PAD to inhibit data transfer to the terminal. The XON and XOFF characters are treated as special characters that interrupt the μP. If the μP receives an XOFF interrupt, the μP inhibits

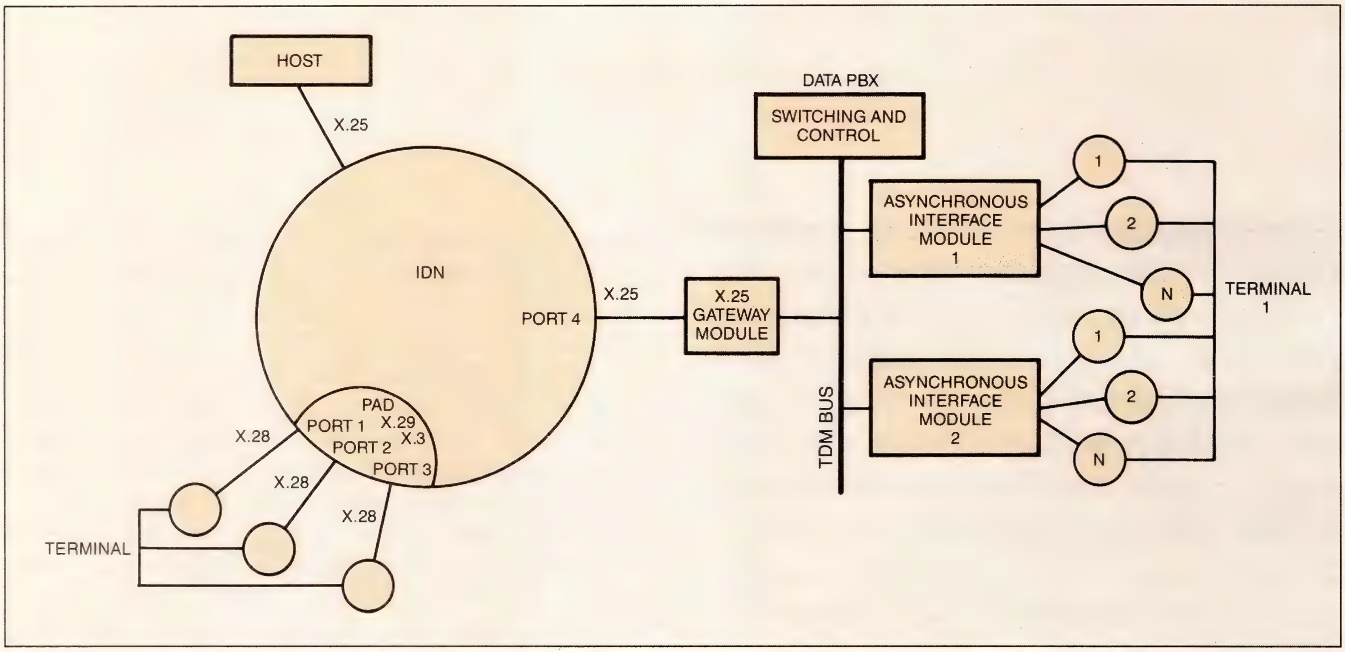


***Fig 1—A gateway is necessary for many terminals** on a PBX to communicate with other devices over an integrated digital network.*

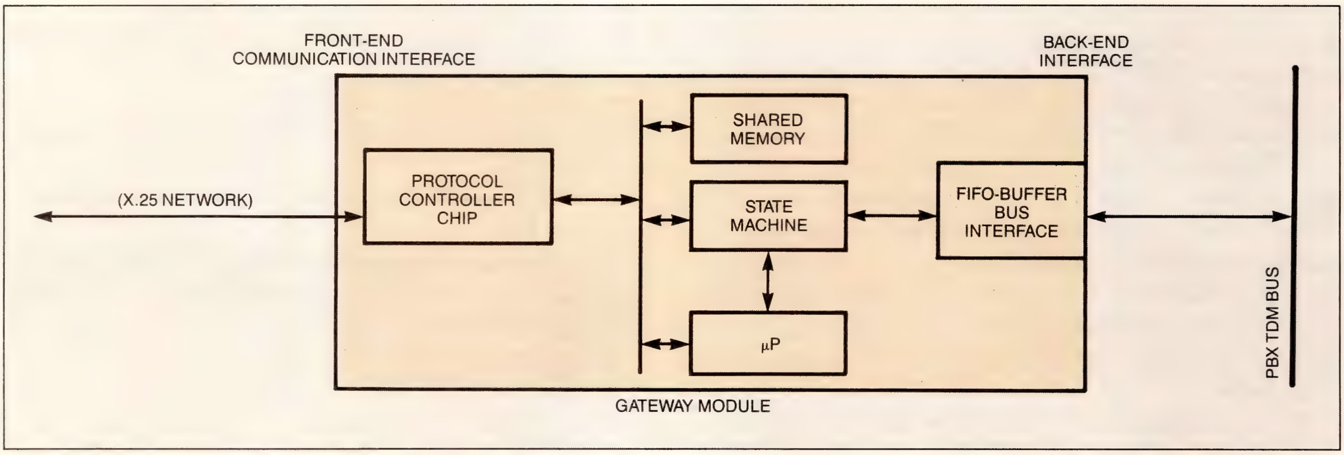


***Fig 2—The state machine offloads many of the tasks** imposed on the μP in the design of a gateway module.*

the data flow until it receives an XON interrupt.

When traffic is heavy in both directions, the PAD must react quickly to accomplish all of its assigned tasks. A PAD design based on a fast state machine is a simple and inexpensive way to avoid congestion.

Fig 3 is a block diagram of a state-machine-based PAD that permits the PAD to transmit data to 128 ports on the PBX link. The μP's primary chore is to initialize the PAD to conform with the characteristics associated with each port. Once initialized, the PAD can transfer data in either direction without intervention by the μP. Therefore, the hardware must maintain the addresses for the transmit- and edit-buffer locations for each of the 128 ports.

The CCITT recommends specific PAD standards

CCITT Recommendation X.3 defines the requirements for a Packet Assembler Disassembler (PAD); therefore, the terms PAD and X.3 are often used interchangeably. The PAD is basically a set of options that allow a non-packet-mode device, such as an asynchronous terminal, to interface to the X.25 packet-switching network. The PAD contains a set of 22 parameters, which create a profile for each of the ports that it services. This profile determines which PAD facilities are in use.

In addition, CCITT Recommendation X.28 establishes the requirements for a PAD to communicate with a start-stop mode terminal. The X.28 specification defines how to log on for service, exchange control information, and exchange data between the two devices. CCITT Recommendation X.29 defines the same information for passing data between a PAD and a packet-mode terminal or between two PADs.

One of the PAD's tasks is to assemble data into packets for transmission over a packet-switching network. In addition, the PAD must disassemble a packet received over a packet-switching network in order to relay the data to a terminal. Because terminals have different communication requirements, the PAD must identify a profile of 22 parameters for each terminal with which it must communicate.

The PAD has two basic modes of operation: a data-transfer mode and a command mode. In the data-transfer mode, the PAD performs the assembly and disassembly tasks. In the command mode, the terminal converses directly with the PAD to initialize and modify some of the 22 parameters. The terminal commands the PAD to enter the command mode by transmitting the PAD-recall character (parameter 1). The following is a brief description of the 22 profile parameters:

1. PAD recall—enters PAD command mode.
2. Echo-mask enable—enables the PAD to echo characters back to the terminal.
3. Data forwarding—sends the packet over the network.
4. Idle timer—sends the packet over the network on timeout value.
5. Terminal flow control—commands XON and XOFF data transfer to the terminal.
6. PAD service signals—PAD sends service signals to the terminal.
7. Break character—defines PAD action upon reception of a break character.
8. Discard output—PAD discards the output to the terminal.
9. Padding after CR—PAD inserts padding characters after CR character.
10. Line folding—specifies the number of characters before each CR.
11. Baud rate—defines the baud rate of a terminal.
12. PAD flow control—commands XON and XOFF data transfer to the PAD.
13. LF insertion—PAD inserts an LF character after a CR character.
14. Padding after LF—PAD inserts padding characters after an LF character.
15. Editing—enables editing during the data-transfer mode.
16. Character delete—defines the character-delete key.
17. Line delete—defines the line-delete key.
18. Line display—defines the line-display character.
19. Edit PAD service signals—defines the PAD's editing service signals.
20. Echo mask—defines which characters the PAD must echo.
21. Parity treatment—PAD performs parity check on received data.
22. Page wait—PAD suspends output after a full-screen display.

The μP's primary chore is to initialize the PAD to conform with a variety of characteristics associated with each port.

The PAD uses four 2k×8-bit static RAMs to store the addresses of the buffer locations. The seven port identification bits on the TDM bus address this buffer management RAM (BMGR). In addition, two 8-bit counters address a 64k×1-bit baud-bit RAM for adjusting to the various port baud rates. The PAD requires two state machines, one for transmitting data and one for receiving it. You can easily implement both state machines with an AM29PL144—a fuse-programmable controller IC from Advanced Micro Devices.

Initially, the μP loads a starting- or current-buffer address (CBA) into the BMGR. The μP loads a 10-bit data word, representing the CBA, into bits 10 through 19 of the 32-bit BMGR. The μP also stores an end-of-buffer address (EBA) in bits 20 through 29 of the BMGR. This implementation permits bits 0 through 9 of the BMGR to be used as a pointer within the current-buffer address (CBAP). A buffer's space can be as large as 1k bytes for each of the 128 ports. The state machine also uses a port-master-control (PMC) RAM, which selectively enables and disables the receive and transmit functions for each port. The μP controls the direction of data transfer by enabling the appropriate bit in the PMC RAM.

After loading the CBA and EBA addresses into the BMGR, the μP sets the port-transmit-enable (TXEN) bit in the PMC RAM, and the state machine assumes the task of transferring the characters for all 128 ports at the appropriate baud rates. The data transfer terminates when the pointer for the current-buffer address equals the end-of-buffer address (CBAP=EBA). At this point, the state machine issues an end-of-buffer interrupt to the μP via the interrupt FIFO buffer.

A baud-bit RAM sets the baud rates

The μP establishes the transfer baud rates by initializing the data in the baud-bit RAM. A 7-bit port counter and an 8-bit slot counter address the baud-bit RAM. The port counter drives the slot counter. A 330-kHz clock increments the port counter every 4.3 μsec, causing the slot counter to increment every 550 μsec (128 ports×4.3 μsec/port=550 μsec). The 550-μsec interval corresponds to the time required to transmit a start, a stop, a parity, and an 8-bit character at 19.2k baud.

Fig 4 illustrates how the bits in the baud-bit RAM

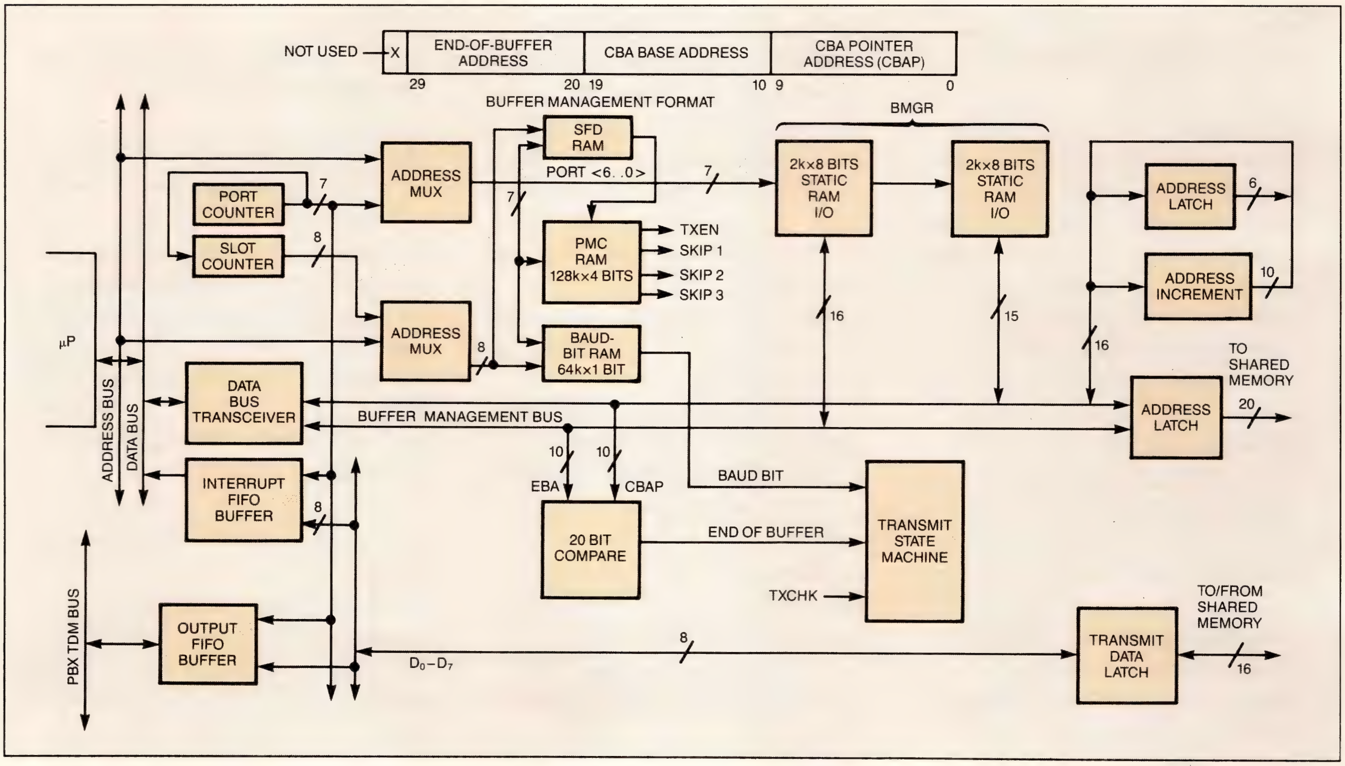


***Fig 3—The transmit state machine interconnects with the buffer-management RAM (BMGR),** the port-master-control (PMC) RAM, and the baud-bit RAM to implement the PAD functions for transmitting data from the shared-memory buffers to the PBX's TDM bus.*

set the baud rates for the individual ports. Each of the 128 ports are partitioned into 256 slots. Because all of the bits for port 0 are set to one, this port transfers data at the maximum baud rate of 19.2k bps. Because the μP sets alternate bits in the allotted slots for port 1, a baud rate of 9600 bps results. With 256 slots available per port, this method of sequentially addressing the baud-bit RAM can produce 256 different baud rates ranging from 19.2k to 75 bps.

When transferring data from the X.25 network to the PBX, the controller IC deposits the data into a transmit buffer and informs the μP that new data is available. The μP sets the TXEN bit in the PMC RAM for the appropriate port and initiates the data transfer. A flow chart for transferring data from the transmit buffer to the output FIFO buffer is shown in **Fig 5.**

Initially, the state machine is in an idle loop. When the LSB of the port counter changes, a circuit sends a transmit-check (TXCHK) command to the state machine on each LSB transition. If the slot counter is enabled, the state machine exits its idle loop and dis-

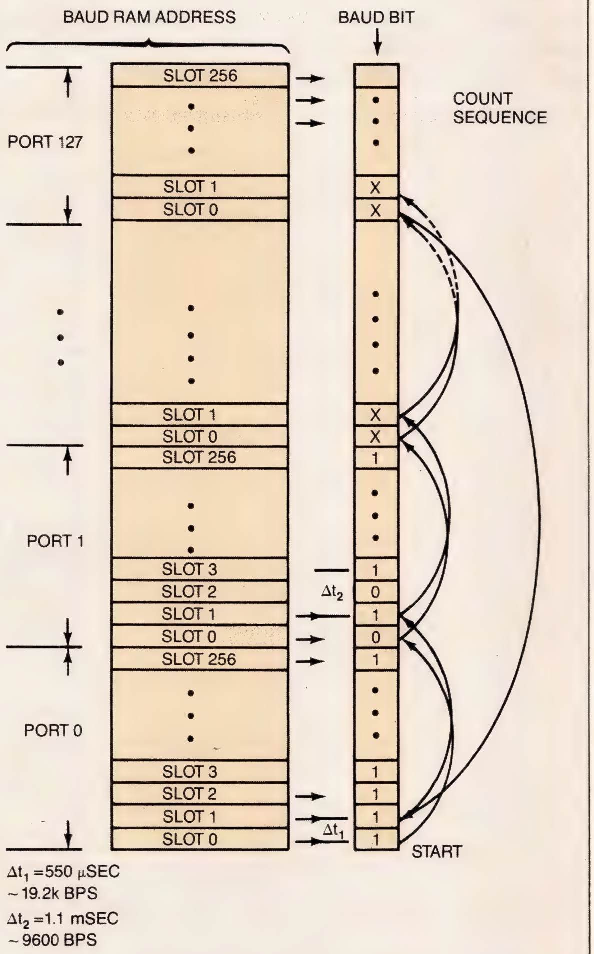


*Fig 4—**By selectively storing ones in the 256 slots** available for each port in the baud-bit RAM, the PAD establishes the port communications for baud rates ranging from 75 to 19.2k bps.*

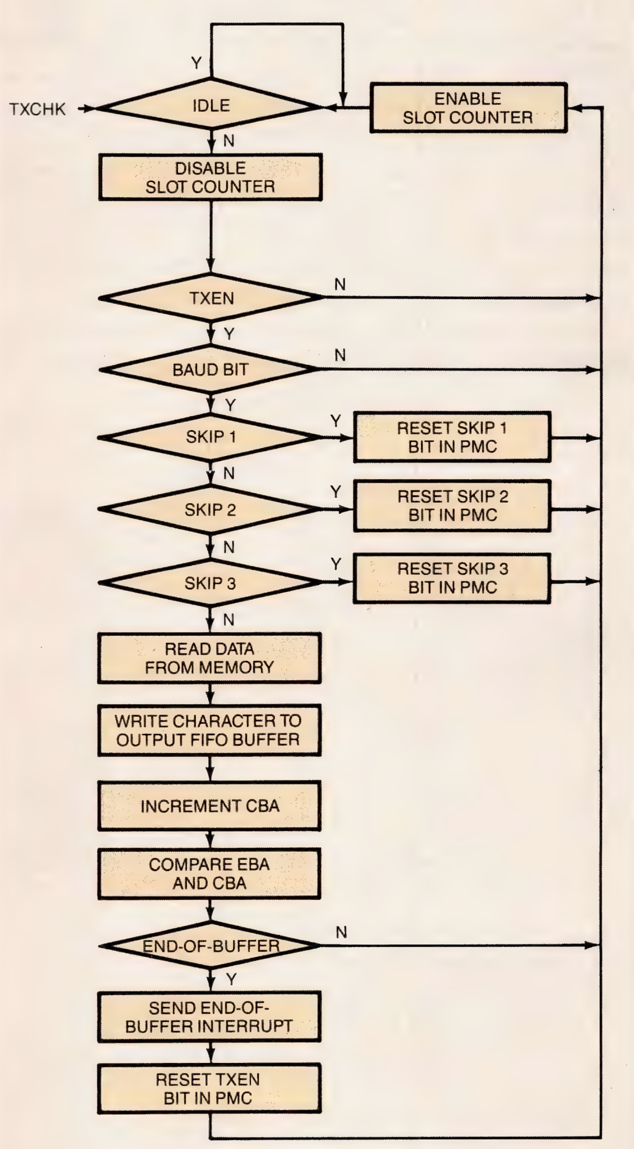


*Fig 5—**The state machine is in an idle state until it receives the TXCHK signal,** indicating that the PAD is servicing a new port. The machine then checks bits in the PMC RAM and the baud-bit RAM before transferring data from the shared-memory buffer to the output FIFO buffer.*

The PAD requires two state machines: one for transmitting data and one for receiving it.

ables any further increments of the slot counter. Next, the state machine determines whether the µP has set the TXEN bit for the current port. If so, the state machine then determines whether a slot bit in the baud-bit RAM is set, thus indicating a valid transmit window.

Special characters increase overhead

The state machine also must have a provision for handling special characters without the FIFO buffers overflowing. For example, when a port operates in a full-duplex mode and is simultaneously receiving and transmitting data, the PAD may be required to send a line-feed character while echoing a carriage-return character. To avoid an overflow condition that could be caused by inserted characters, the PMC RAM has three skip bits—SKIP1, SKIP2, and SKIP3—to inhibit data transfer from the shared-memory buffer.

The address lines for the special-feature-detect (SFD) RAM consist of the port-identification bits and the receive data bits. If the SFD RAM determines that the incoming character requires echoing, it sets the appropriate skip bits in the PMC RAM. If any of the three skip bits in the PMC are set, the state machine does not transfer data from the shared memory during the time slot. This time delay permits the PAD to insert additional characters in the data stream without causing an overflow condition.

When transmitting a character from the transmit buffer, the state machine loads the 10-bit CBA and the 10-bit CBAP into a 20-bit latch. After latching the 20-bit address, the state machine issues a read command to transfer the data to the output FIFO buffer. Because the BMGR uses 8-bit static RAMs, the least-significant 16 bits must be used to increment the pointer address. The state machine latches the upper six bits of this 16-bit word and increments the lower 10-bits in an address counter. It then writes the resulting 16-bit word back into the BMGR. If the 20-bit comparison circuit detects that the new CBAP and the

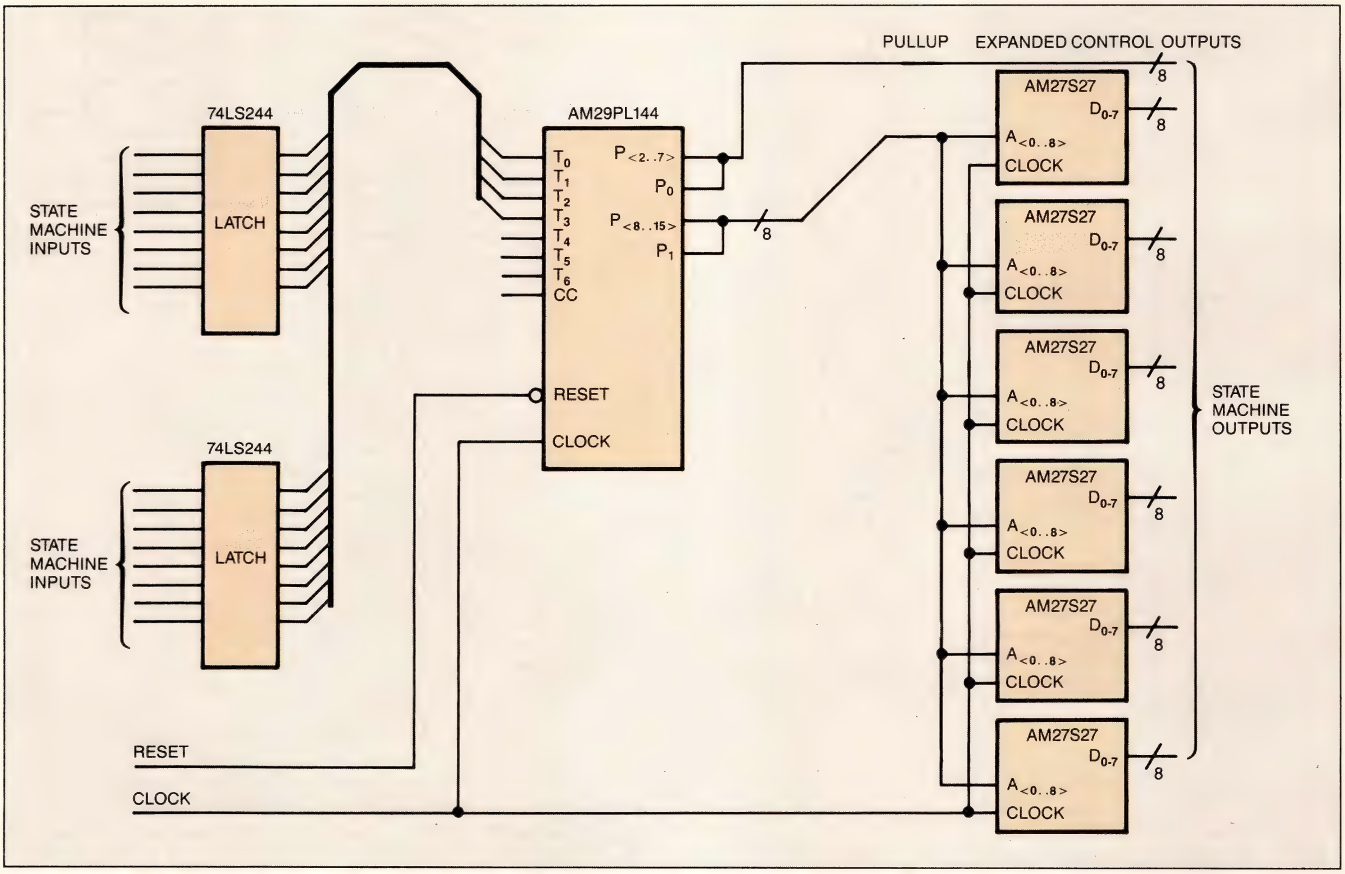


Fig 6—You can implement both the transmit and the receive state machines *by using an AM29PL144 fuse-programmable controller from AMD. Using this device with AM27S27 registered PROMs greatly expands the number of control outputs.*

EBA are equal, the state machine sends an end-of-buffer interrupt to the μP. The state machine then resets the TXEN bit in the PMC RAM, thus disabling further data transfers from that port.

You can expand the number of output control lines by placing the AM29PL144 registered PROM in its external mode and combining it with a series of registered PROMs. In the external mode, the AM29PL144 places the microinstruction address on its output lines labelled P_8 through P_{15} and P_1. A state-machine design using these output lines as address lines for the registered PROMs is shown in **Fig 6.**

The PAD must check each incoming character against a particular port's profile, and this routine is compute-intensive—particularly when the direction of data flow is from the PBX to the X.25 network. With a large number of ports to service, the PAD protocol can become a gateway bottleneck. By implementing the character-checking task in hardware, the μP is free to perform high-level PAD functions until interrupted by the detection of a special character. The block diagram of the PAD performing the receive functions is shown in **Fig 7.**

The SFD RAM is a 64k × 12-bit RAM. The state machine interfaces with the SFD RAM to determine whether an incoming character is a special character before writing data to the shared memory buffer. If the state machine detects a special character, the 32 × 8-bit SPCL Echo PROM loads the interrupt FIFO buffer with a byte informing the μP to take control of

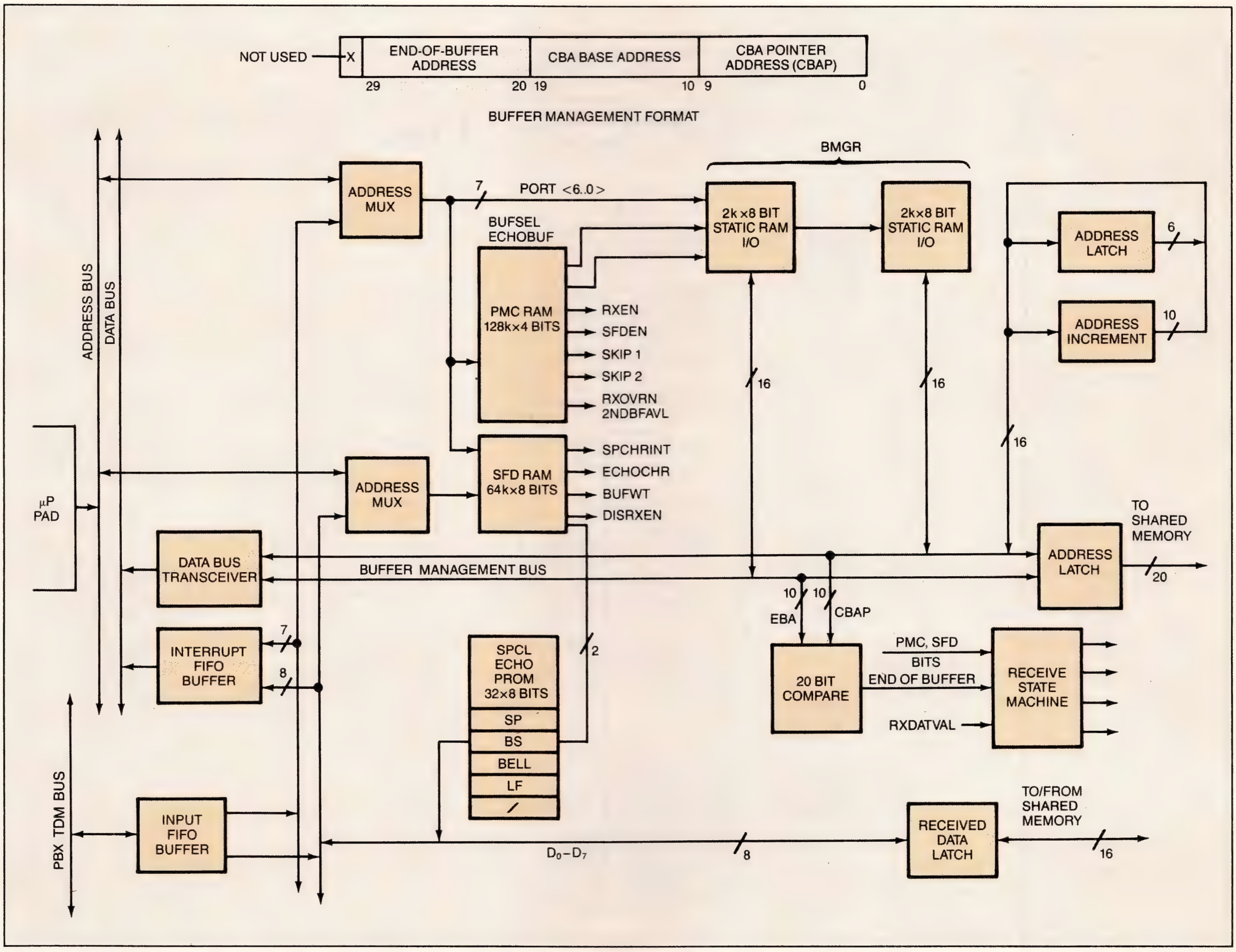


Fig 7—The receive state machine must interface with the BMGR, the PMC RAM, and the special-feature-detect (SFD) RAM to decide if any preliminary action is required before transferring data to the controller IC.

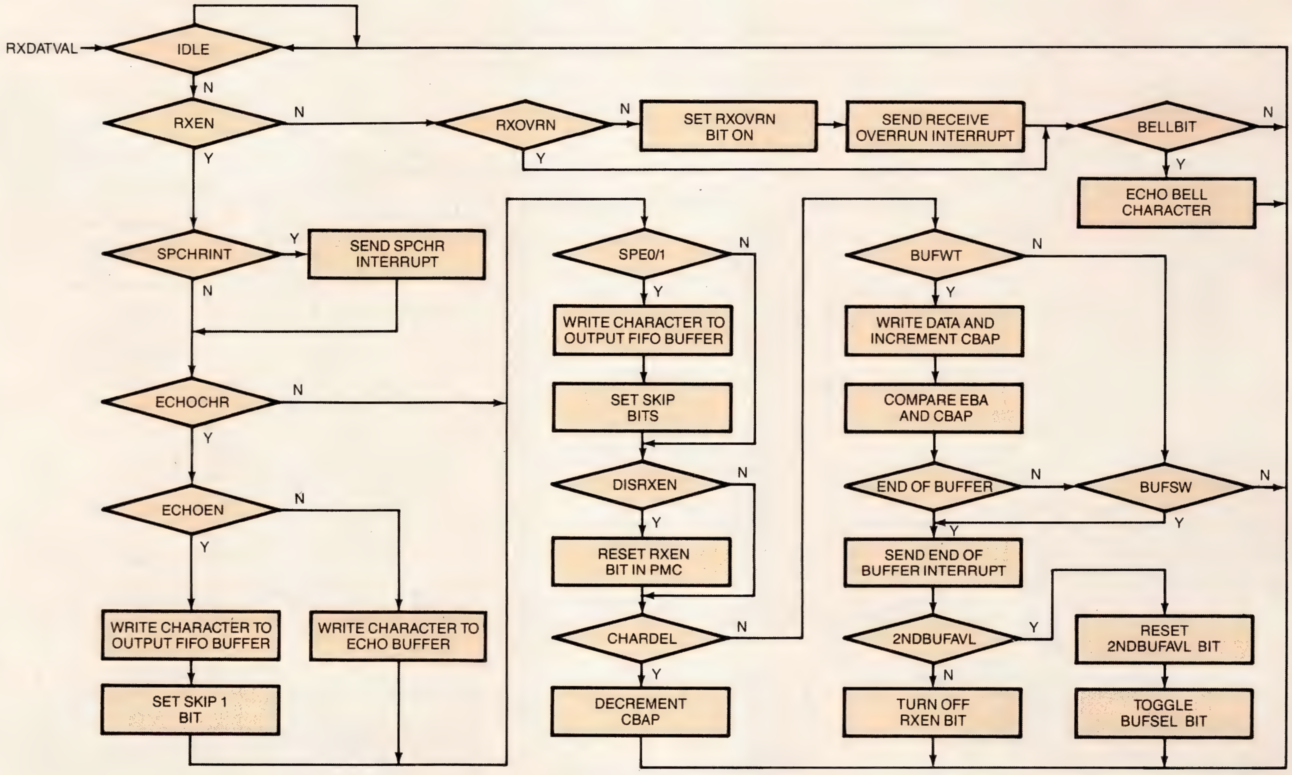
The state machine uses a port-master-control RAM, which selectively enables and disables the receive and transmit functions of each port.

the edit buffer. **Fig** 8 is a flow diagram of the state machine transferring data from the TDM bus to the shared-memory buffer.

Extra space handles contingencies

Generally, only the packet-forwarding character (parameter 3) interrupts the μP. In these instances, the μP allocates a new edit buffer for the incoming data and makes the data in the current-edit buffer available to the packet assembler. The packet assembler builds the packet header and passes the packet to the controller IC. Essentially, the PAD overhead consists of buffer management.

In some instances, however, the shared-memory capacity must be large enough to contain dual-edit buffers. For example, the input FIFO buffer might overflow when file transfers take place or when a terminal uses the CR character as a packet-forwarding character. During heavy traffic, there is no latency time between characters for the μP to load a new edit-buffer address into the BMGR. Therefore, the PAD requires a dual-edit-buffer architecture to eliminate this potential problem. A dual-buffer architecture lets the μP preload the BMGR to address an auxiliary edit buffer while data transfers take place in the active edit buffer. The state machine uses two outputs from the PMC RAM, the BUFSEL and AUXBUFAVL bits, to select the available edit buffer (see **box,** "The PMC RAM



SPECIAL-CHARACTER RAM DEFINITIONS

SPCHRINT	SPECIAL-CHARACTER INTERRUPT
BUFWT	WRITE TO THE BUFFER
DISRXEN	DISABLE THE RECEIVE-ENABLE BIT
ECHOCHR	ECHO THE CHARACTER
CHARDEL	DELETE THE CHARACTER
ECHODIS	DISABLE THE ECHO FEATURE
ENCHRINT	ENABLE THE INTERRUPT ON THE NEXT CHARACTER
BUFSW	SWITCH TO AN AUXILIARY BUFFER
SPE0/1	SPECIAL ECHO BITS 0 AND 1

Fig 8—The receive state machine is in an idle state until it receives an RXDATVAL command, *indicating that valid data is available in the input FIFO buffer. The receive state machine must then check each character against its port profile to see what action is required.*

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The state machine must have a provision for handling special characters without overflowing the FIFO buffer.

affects the course of action").

In other instances, the PAD requires an echo buffer for saving characters when the automatic-echo feature (parameter 2) is enabled. For example, if a terminal sends an XOFF control character to the PAD and continues to type ahead, these characters must be saved in the echo buffer. The PAD retransmits the saved characters to the terminal at a convenient time once the PAD receives the XON control character. The state machine monitors the ECHOEN bit in the PMC RAM to decide whether to transfer data to the echo buffer.

The profile parameters permit the PAD to edit data in the current edit buffer. Parameter 15 enables the editing features. The state machine implements the character-delete feature (parameter 16) by loading the CBA pointer into the buffer-address counter, decrementing the counter, and writing the result back into the CBA pointer location in the BMGR. In order to

The PMC RAM affects the course of action

The state machine utilizes the port-master-control (PMC) RAM to determine a course of action for each of the ports on the TDM bus. Initially, the μP programs the 128×12-bit RAM with data for each port. A multiplexer, which the μP controls, selects either the 7-bit initialization address from the μP or the 7-bit port-identification bits on the TDM bus as the RAM's seven address lines. The 11 output bits used by the state machine are

1. RXEN—receiver enabled. The state machine monitors this bit to determine whether to transfer data from the input FIFO buffer to the shared-memory buffer. If data is present and this bit is not set, the state machine issues an overrun-interrupt signal.

2. RXOVRNINT—receiver-overrun interrupt. The state machine checks this bit before issuing the overrun-interrupt signal. If this bit is set, the state machine discards the received data. Otherwise, the overrun-interrupt signal sets this bit.

3. AUXBUFAVL—auxiliary buffer available. Because the gateway provides a dual-buffer architecture to prevent data overruns, the state machine must check this bit upon the detection of a special character and when an end-of-buffer condition occurs. This bit determines which buffer to select.

4. BUFSEL—buffer select. If the AUXBUFAVL bit is set, the state machine sets the BUFSEL bit to transfer data to the auxiliary buffer and resets the AUXBUFAVL bit.

5. SKIP1—skip a transmit time slot. This bit prevents a possible data overflow condition. A situation may arise in which the PAD must echo a received character back to the terminal while the PAD is transferring data from the shared-memory buffer to the same port. The state machine sets this bit to prohibit a data transfer during this time slot.

6. SKIP2—skip a second transmit time slot. The state machine enables this bit to inhibit data transfer from the shared-memory buffer for two time-slot periods. The bit prevents a possible overflow condition when the PAD must echo a CR character and add an LF character.

7. SKIP3—skip a third transmit time slot. This bit operates in a similar manner as the previous skip bits. It prevents a possible overflow condition when the PAD must delete a character. The PAD must transfer a backspace-space-backspace sequence to the terminal to accomplish this editing feature.

8. TXEN—transmitter enabled. The state machine monitors this bit before transferring data in the shared-memory buffer to the output FIFO buffer on the TDM bus.

9. BELLBIT—Bell-character enable. If the μP initializes this bit, the PAD echoes a bell character each time it receives a character that generates an overrun-interrupt signal.

10. ECHOEN—echo enable. Enables the PAD to echo characters back to the terminal.

11. INTNXTCHR—interrupt on next character. If this bit is initialized, the next character received from the specified port generates a special-character interrupt. The next character also disables this bit.

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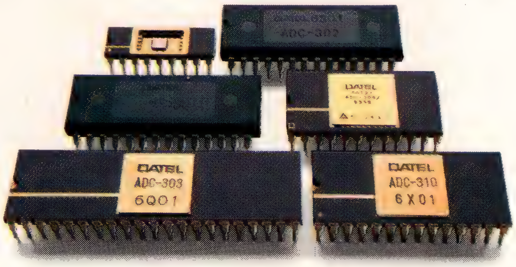

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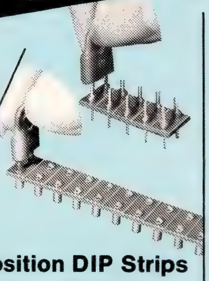

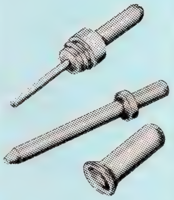

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These Aries .040 (1,01) diameter shorting plugs and jacks are gold or tin plated beryllium copper pins or contacts in a glass filled thermoplastic body, UL94VO rated.

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Female socket and two styles of male pins are available for staking into p.c. boards. Socket contacts are gold plated beryllium copper.

See EEM Vol. C, pgs. 1185-1190

CIRCLE NO 73

erase the character on the terminal's display, the PAD must echo a backspace-space-backspace sequence to the terminal.

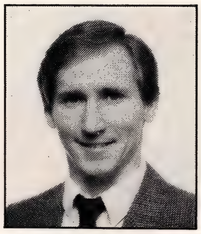
You can best implement the line-delete feature (parameter 17) by using a routine resident in the µP. If the PAD receives a line-delete character, it generates an interrupt signal to the µP. Upon interruption, the µP calls a routine that calculates the appropriate number of backspace-space-backspace sequences required to erase the entire line and transmits them to the terminal. Because this feature is seldom used, the CPU overhead is negligible.

The state-machine architecture handles the majority of the throughput requirements for the X.3 PAD protocol; however, some infrequent services are easier to execute by using a subroutine for the µP. Parameter 9, which specifies that a number of padding characters be inserted after a CR character, is one of these services. In addition, the µP must reassign the definitions of certain special characters when switching between the data-transfer and command modes. Because these chores occur infrequently, the extra burden on the µP is insignificant. EDN

Acknowledgments

The author would like to thank Jim Papke, John Scarpelli, and Nick Scordalakes for their contributions to this article.

Author's biography



Brian Bennett is a senior engineer for McDonnell Douglas Electronic Systems Co in Huntington Beach, CA. His current project is RISC-based µP systems. Brian previously worked for Computerbase. He holds a BSEE from California Polytechnic State University, San Luis Obispo, and is currently enrolled in the MSEE program at the University of Southern California. In his spare time, which is shared with his wife and two daughters, he enjoys volleyball, tennis, softball, and skiing.

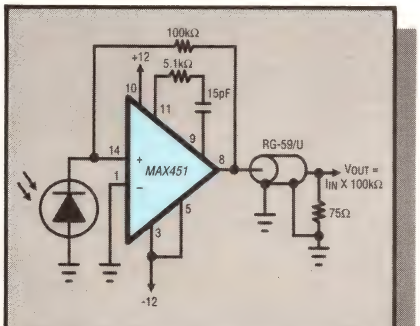
Article Interest Quotient (Circle One)
High 488 Medium 489 Low 490

MAXIM
DESIGN NEWS

Analog Design Insights from Maxim Integrated Products March '89

70MHz CMOS Video Amplifiers Tame Losses in Wideband Circuits

Digital techniques are frequently used for video processing. However, we live in an analog world and the distribution of video signals is usually handled by analog means. Teleconferencing cameras, video routing, video crosspoint switches, and video attenuators all need zero insertion loss, low input capacitance and 75Ω drive capability. Maxim's MAX450 - 457 family of CMOS video amplifiers/multiplexers exhibit low differential phase and gain errors, up to 70MHz video bandwidths, and provide 75Ω cable drive.



PIN Diode Transimpedance Amplifier

They work well in standard op-amp configurations, but they are optimized for high frequency video applications. The MAX450/1 video amplifiers work from ±8V to ±15V supplies. They can drive 75Ω loads directly to a guaranteed ±2V minimum swing at 1MHz (typically 3.5V with ±12V supplies). These devices have very high input impedance, typically 10MΩ. Bias current for the two is typically 0.4nA with a guaranteed 1nA max. for the MAX451. The amplifiers can be used for vidicon preamps or photodetector preamps in fiber optic systems requiring up to 10MHz bit rates. For gains greater than 20, the amplifiers do not require any compensation. Gains less than 20 require two RC networks. These networks optimize the pulse response, and can be used to compensate for skin effects and the capacitive loading of long cables used in video distribution applications.

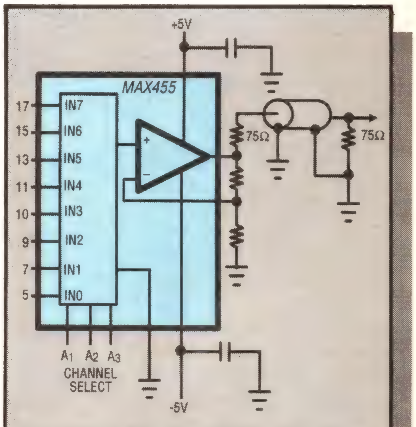
Multiplexer-Amp Combo

For higher bandwidth applications, up to 70MHz, Maxim's MAX452/3/4/5/7 devices offer significant performance improvements over discrete solutions.

These devices operate from ±5V and drive ±2V into a back terminated 75Ω cable. The MAX455 is a 50MHz, 250mW, eight channel multiplexer with onboard amplifier. Other versions have four channels (MAX454) and two channels (MAX453) as well as the base video amplifier MAX452. The new MAX457 is a dual video amplifier that has a 70MHz bandwidth.

Previous high bandwidth solutions required two separate chips, like a 100MHz CMOS multiplexer and 100 to 300 MHz bipolar or hybrid amplifier. This approach was both expensive and difficult to implement. The amplifiers used were usually difficult to stabilize near unity gain and the layout and interconnection of components was critical. The wideband multiplexers were designed with low ON resistance, typically 50 to 75Ω, to drive low impedance 75Ω cables. This produced an insertion loss that usually required signal amplification to restore the level back to normal video standards. The low impedance of the switches used in the multiplexers resulted in high channel capacitance, as much as 50pF, which limits the pass bandwidth to 50-100MHz, because of the RC rolloff. Even if lower capacitance switches were used, the stray capacitance connecting the multiplexer and amplifier reduced the bandwidth.

The two chip multiplexer-amplifier combination presented many problems for the video designer. CMOS multiplexers are ideal for video switching with minimal power consumption, and bipolar op-amps are best for gain bandwidth products. If an all bipolar chip with diode bridge multiplexer switches were designed, the device would consume a lot of power, whereas an all CMOS chip of conventional design would be too slow. The monolithic CMOS MAX453/4/5 architecture significantly improves the performance of the combination by using a unique approach. The approach was to make a relatively low open-loop gain amplifier look like a multistage op-amp when driving cable impedance, while delivering single stage gain to prevent excessive phase shift and oscillation. This was achieved by designing an amplifier that eliminated the need for phase compensation. At the same time, the amplifier was optimized for gain-bandwidth products without the oscillation at low-loop gain. The device bandwidth is improved by a factor of 2-10. The voltage gain of the amplifier used in the MAX452/3/4/5/7 devices is proportional to the load impedance.



MAX455 8 Channel 50MHz Mux/Amp

In addition, the node connecting the multiplexer and amplifier is not brought out on the MAX453/4/5. This keeps the parasitic capacitance to a minimum. The input impedance of the multiplexer amplifier combination is high, typically 100,000MΩ. The ON channel input capacitance is 7pF, 3.5pF for an OFF channel.

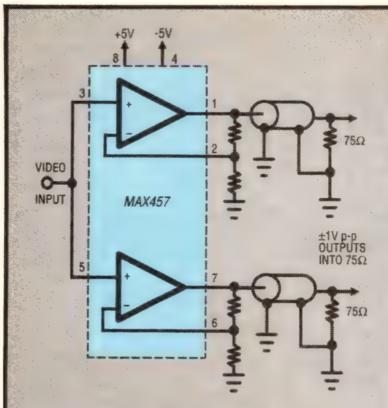
VIDEO PRODUCTS

Video Amplifiers and Buffers

Part #	Function	Bandwidth	Slew Rate (V/µs)	Features	Price (1000- up)
MAX450	Video Op Amp	10	70	Drives ±2V into 75Ω	$2.28
MAX451	Video Op Amp	10	70	1nA max. I_{BIAS}	5.19
MAX452	Video Op Amp	50	150	Drives ±1V into 75Ω	2.67
MAX453	Video Mux/Amp	50	150	2 Channel input Mux	3.99
MAX454	Video Mux/Amp	50	150	4 Channel Input Mux	5.32
MAX455	Video Mux/Amp	50	150	8 Channel Input Mux	8.86
MAX457	Dual Video Amp	70	150	Drives ±1V into 75Ω	4.45
BB/AD3554	Video Op Amp	1700	1000	100mA, High Gain	44.20
MAX460	Video Buffer	100	1500	100mA, Drives 75Ω, Low I_B and C_{IN}	$18.80
LH0033	Video Buffer	100	1500	100mA Drives 75Ω	13.12
LH0063	Video Buffer	300	6000	200mA, Drives 50Ω	23.51
BB3553	Video Buffer	300	6000	200mA, Drives 50Ω	22.51

Video Switches and Multiplexers

Part #	Function	$R_{DS\ ON}$	Signal Range	Features	Price (1000- up)
MAX310	1 of 8 Mux	250Ω	+12V to -15V	70dB Isolation at 5MHz	$7.59
MAX311	2 of 8 Mux	250Ω	+12V to -15V	70dB Isolation at 5MHz	7.59
IH5341	Dual SPST Video Switch	75Ω	+15V to -15V	70dB Isolation at 5MHz	2.66



MAX457 Dual Video 70MHz Distribution Amplifiers

The multiplexer-amplifier RC rolloff is typically 50MHz when driving a 75 Ω load at unity gain. A ' T ' section is used for each of the switches in the multiplexer to attain high OFF isolation and interchannel isolation, typically 70dB at 4MHz. This high isolation is impaired if the layout of the devices is not done with care. A groundplane is necessary in most applications and unused pins must be grounded to provide internal interchannel shielding.

±12V Video Routing

Video circuits that need to switch or route higher level signals (such as crosspoint systems) can take advantage of the MAX310/311 video multiplexers. They guarantee both 36V single supply operation and operation from ±4.5V to ±16.5V supplies. The MAX310 is a 1 of 8 multiplexer while the MAX311 is a 2 of 8 (4 channel differential). Power consumption is typically just 1.2mW. The control inputs are fully TTL and CMOS compatible. Decoding is standard BCD format with an Enable input to simplify cascading of devices. Each switch has guaranteed break-before-make to prevent momentary shorts between inputs when changing multiplexer channels. The MAX310/311 are bilateral in that they can be used backwards, as demultiplexers, with no loss in performance. The isolation of each OFF channel to output is guaranteed to be better than 66dB at 5MHz. The MAX311 is particularly useful in differential switching of coaxial cables where the signal and cable ground returns are switched for each signal source. This minimizes the cross talk between channels by keeping ground return currents from affecting other video sources.

Watch the Layout

High frequency circuits suffer from the influences of poor circuit layout and inadequate packages used for the devices. Conventional plastic DIPs act like lowpass filters for video signals and can compromise the performance of circuits in the 50MHz range. Surface mount packages such as SOIC have reduced parasitics. Similarly, surface mount resistors and capacitors also exhibit lower lead inductance, resistance, and capacitance. To maximize your performance, the following suggestions are offered as a guideline:

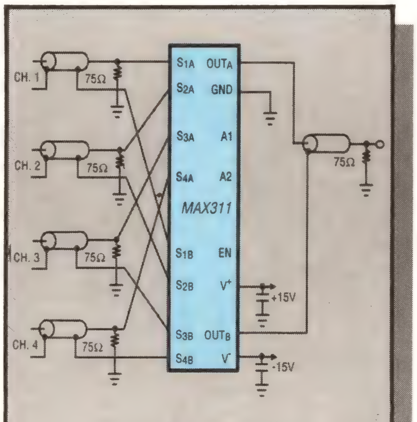
1. Use a ground plane. It provides a shielded, low resistance, low inductance ground reference and reduces undesirable high frequency coupling.

2. Avoid IC sockets. The increased inter-lead capacitance can degrade bandwidth and increase feedback capacitance.

3. Keep input and output connections short. This results in a more compact physical layout and minimizes parasitic coupling.

4. Minimize capacitance. The capacitance from output to input of amplifiers should be kept to a minimum to reduce the possibility of oscillations.

5. Keep PCB traces wide. Supply and output traces should be kept as wide as possible to minimize inductance and resistance.



Coaxial Cable Switching

Video Parameters Reviewed

The dynamic performance of video amplifiers is more important than the DC performance. Many tradeoffs are made to optimize AC performance. The dynamic performance of video amplifiers is expressed by three different parameters: bandwidth, slew rate, and settling time.

Bandwidth is a measure of the highest frequency signal that the amplifier can pass. This bandwidth is usually specified at some specific gain (usually a gain of one or two).

Slew Rate is the speed at which the amplifier can slew its output over a specified output signal range, expressed in V/µs.

Settling Time is the time that it takes the amplifier to settle within some error band around a final value after a step change from some other value.

In some video applications differential phase/gain errors are also important parameters. For example, these parameters are particularly important in television applications.

Differential Phase error is probably the single most visually apparent distortion in a television video system. Color information is contained in the 3.58MHz color sub-carrier of the NTSC video standard (4.43 MHz for the PAL standard). By modulating both the phase and amplitude of the carrier, the color and hue information is transmitted. The color carrier "rides on" the luminance signal, a much lower frequency signal that contains the black and white information. A reference burst of carrier occurs at the beginning of each line scan, after the line sync pulse. As the scan proceeds, the luminance signal changes from black to white through variations of gray. The chrominance information is added to the luminance information to create a composite video signal. The variation of the luminance level can cause phase shift in the color carrier. In turn, this phase shift causes color errors in the video image. Video amplifiers with significant differential phase error induce a color error that changes the hue between light and dark regions of the video picture.

Differential Gain is quite similar to differential phase. An amplitude reference occurs at the beginning of each line (black level). As the luminance level varies during the line scan, the high frequency gain may vary, which causes color signal amplitude errors. Large amplitude errors can cause significant color distortions.

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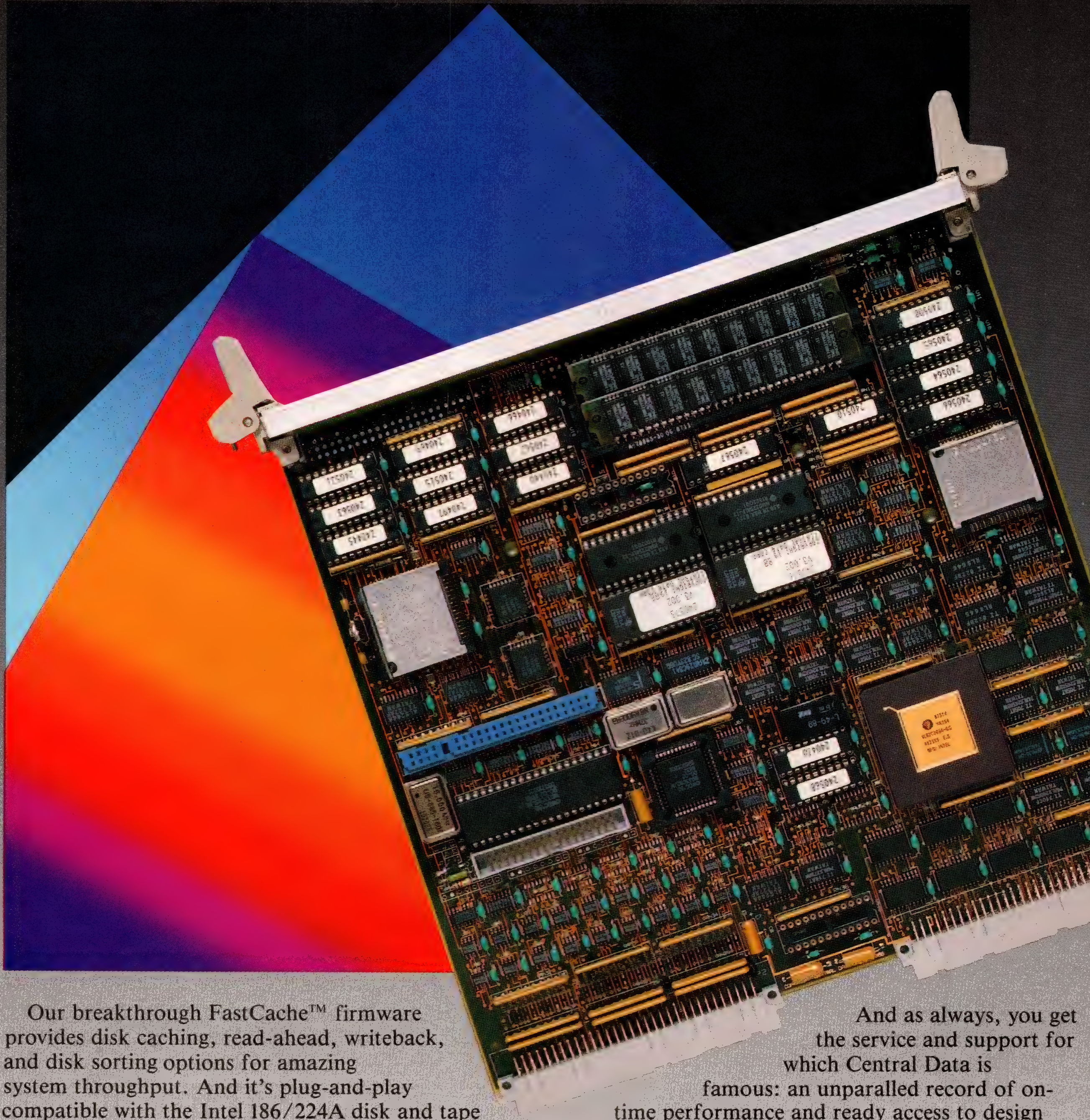

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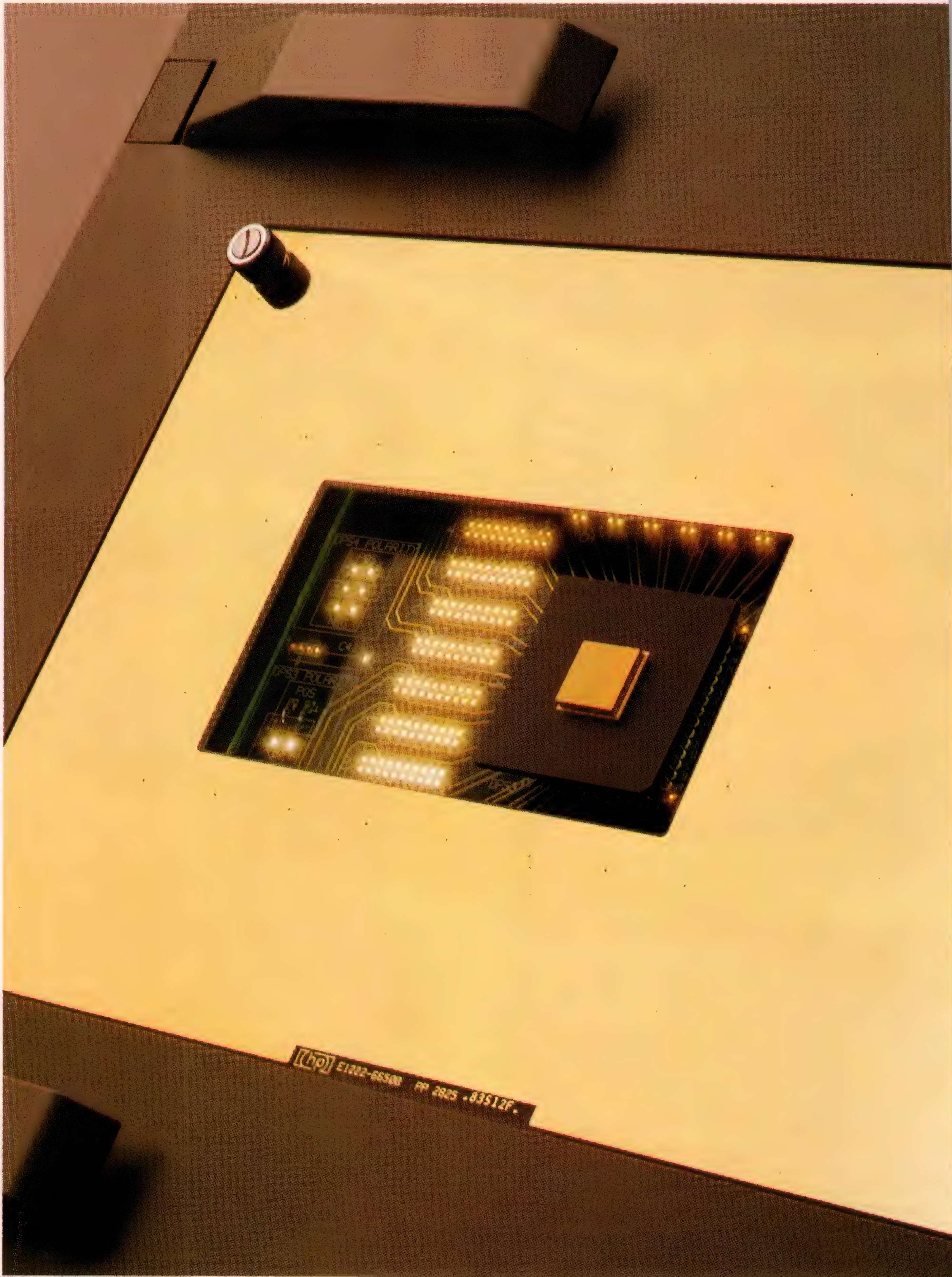

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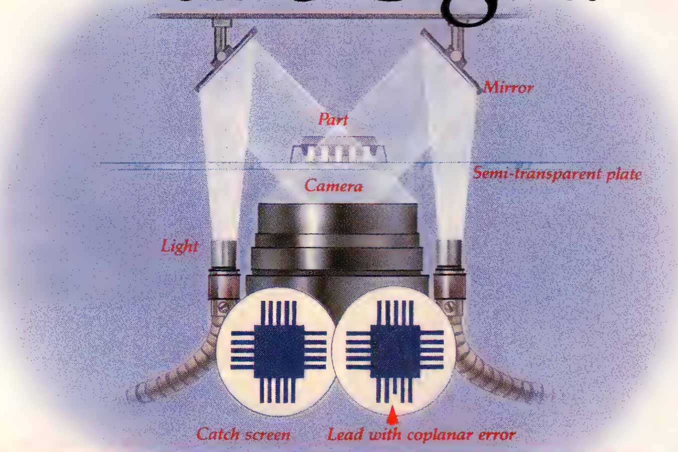

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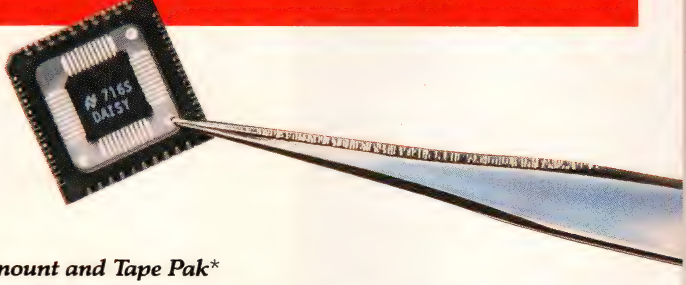

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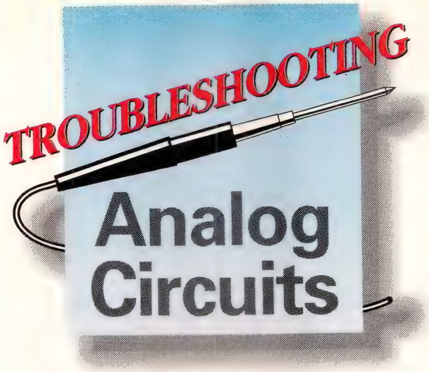


PART 5

Follow simple rules to prevent material and assembly problems

In addition to your choice of components, the materials you use to assemble your circuit will have an impact on how well it performs. This article, part 5 of a 5-part series on troubleshooting passive components, covers what you need to know to solve the occasional problems caused by pc boards, solder, connectors, wire, and cable. Also covered is pc-board layout—a poor layout can cause more than occasional problems; it can completely determine how well your circuit works.

Robert A Pease, *National Semiconductor Corp*

Some of the topics discussed in this troubleshooting series so far may have seemed obvious. But far too often it is this information that engineers overlook, and it is this information that can make troubleshooting so much easier. So, be careful not to overlook the obvious. Don't assume that your pc-board materials or layout don't matter or that wire characteristics don't differ; you'll find that pc boards, connectors, wire, and cable cause problems when you least expect it.

First of all, the use of the term "printed-circuit board" is a misnomer; these days, almost every board is an etched-circuit board. But I'll continue to use the abbreviation "pc board" because it's a familiar term.

There are six basic troubles you can get into with pc boards:

- The board is the wrong material.
- The quality of the vendor's board is so bad that there are opens or shorts in the board or, worse yet, intermittent connections in the plated-through holes.
- The foil starts to peel off the board because of mistreatment.
- You were so concerned with cost that you neglected to specify a layer of solder mask; you ended up with a board full of solder shorts.
- The surface of the board is leaky or contaminated.
- Your circuit layout is such that signals leak and crosstalk to each other or controlled-impedance lines are interfering, thus causing reflections and ringing.

Avoid pc-board problems at the outset

The fixes for these problems, and ways to avoid them in the first place, are fairly straightforward:

These days, the G10 and G11 fiberglass-epoxy materials for pc boards are quite good and reasonably priced. Trying to use phenolic or "fishplate" is not economical in most cases. Conversely, a special high-temperature material or an exotic material or flexible substrate may be justifiable. If you don't have an ex-

Don't overlook problems that can be caused by pc boards, connectors, and cable; they are often the source of your circuit's trouble.

pert on these materials, the pc-board maker or the manufacturer of the substrate material can usually provide some useful advice. (See **Table 1** for a comparison of pc-board materials.)

In some RF applications, phenolic material has advantages over glass epoxy; it has a lower dielectric constant and superior dimensional stability. And for ultrabroadband oscilloscope probes, glass epoxy has a definite disadvantage due to mediocre dielectric absorption, especially if the epoxy has not been properly cured.

As for quality, there is almost never an excuse for buying your boards from a vendor whose products are of unknown quality. "Low cost" would be one poor alibi; "Can't get acceptable delivery from our normal vendor," would be another. One time, to meet a rush contract, we had to build circuits on boards made in our own lab facilities. I had never had trouble before using these boards for prototyping, so I was surprised when I began the troubleshooting and found that an apparently good board occasionally had a short between two buses.

Close inspection with a magnifying glass showed a hairline short about 3 mils wide, which was caused by a hair that fell onto the artwork. You would never ask a printed-circuit foil that narrow to carry 20 mA, but this narrow short would carry 200 mA before blowing out. Similarly, we found hairline opens: The ground bus was broken in two or three places by a tiny 4-mil gap, just barely visible to the naked eye. After several hours of fiddling around, opening shorts, and shorting opens, we vowed not to be caught by such poor workmanship again.

As for the third problem, don't let hamfisted engineers or technicians beat up a good pc board with the overenthusiastic or misguided application of a soldering iron. That's sure to lift the foil.

Solder mask, the subject of the fourth problem, is almost always worthwhile, as many people have learned. Without it, the admirable tendency of solder to bridge things together, which is wonderful in most instances, becomes disastrous.

When a pc board comes from its manufacturer, it is clean and exhibits high impedance. Sometimes a board starts out leaky, but normally a board doesn't begin to leak until you solder it or wash it with a contaminated solvent—the fifth problem. (For a description of two methods for testing leakage, see **box,** "Looking for leakages.").

Recently, a customer had a problem with a design using an LM317 regulator in which the impedances were fairly low. After just a few minutes of operation, the output of the LM317 would start drifting badly. The cause turned out to be not the LM317 or the

TABLE 1—PC-BOARD LAMINATE MATERIALS

TYPE	MANUFACTURER	DIELECTRIC CONSTANT (AT 1 MHz)	DISSIPATION FACTOR (AT 1 MHz)	VOLUME RESISTIVITY (MΩ-cm)	SURFACE RESTIVITY (MΩ)	MAXIMUM TEMPERATURE (°C)	COMMENTS
XXXPC	GENERIC	4.1	0.032	5×10^6	5×10^4	+125	LOW COST, PAPER-BASED PHENOLIC; POOR MECHANICAL STRENGTH
CEM-1	GENERIC	4.5	0.025	1×10^8	5×10^7	+130	STANDARD, ECONOMICAL
CEM-3	GENERIC	4.7	0.020	1×10^8	5×10^7	+130	SIMILAR TO CEM-1 BUT CAN BE PUNCHED
G-10	GENERIC	4.75	0.023	5×10^8	4×10^8	+130	COMPARABLE TO CEM-3
F4486	OAK	3.5	0.02	1×10^9	3×10^6	N/A	FLEXIBLE
FR-4	GENERIC	4.9	0.018	1×10^8	5×10^7	+130	SIMILAR TO CEM-3 BUT FIRE RETARDENT PER UL-94-V-0
GT-522	KEENE	2.5	0.0010	1×10^7	1×10^7	+260	TEFLON IS GOOD FOR HIGH TEMP, HIGH SPEED
GX-527	KEENE	2.5	0.0019 (AT 10 GHz)	1×10^7	1×10^7	+260	CHARACTERIZED FOR HIGH FREQUENCY
HI-3003	TECHNOPLY	4.5	0.020	3×10^7	5×10^6	+250 (10,000 HOURS)	POLYIMIDE
3003-QUARTZ	TECHNOPLY	3.6	0.004	5×10^9	8×10^7	+250 (10,000 HOURS)	COMPARABLE TO CEM-3

resistors or capacitors, but the flux buildup where the board hadn't been washed after soldering. In this case, the impedance of the scorched flux was as low as 500Ω when measured across a 0.1 × 1-in. area of the pc board. So, even if you are not trying to achieve $10^{12}\Omega$ of leakage resistance, you should still observe rudimentary standards of cleanliness, or even your simplest circuits won't work right.

Similarly, one of our pc boards designed for a S/H circuit was yielding $10^{11}\Omega$ of leakage resistance, which was unacceptable. We tried cleaning the board with every organic solvent but had no luck. Finally, I took a few boards home and set them in the dishwasher along with the normal charge of Calgonite. After a full wash and rinse cycle, I pulled out the boards, banged them to shed most of the water beads, and set them in my oven to dry at 160°F. The next day, they checked out at the more acceptable value of $10^{13}\Omega$. I have used this technique several times on leaky pc boards and sockets, and it works surprisingly well.

Make sure the designers of your pc board keep a list of rules to avoid troubles. For example, if your circuit has a high-impedance point and you suspect leakage might be a problem, don't run that high-impedance trace beside a power-supply foil—guard it with a stripe of ground foil between the two. A dozen times I have heard an engineer say, "The resistivity of this glass-epoxy material is $10^{14}\Omega$-cm, so you can't possibly have a resistivity of $10^{12}\Omega$ from your summing point to the rest of the world . . . . " Then, I demonstrate that the measured impedance is typically a lot more than the specifications say, but I agree that I wouldn't dare count on that fact. So, I guard the summing point to ground with a grounded foil surrounding the critical nodes on both the top and bottom of the boards.

With the addition of these grounds, the circuit can perform well even under worst-case humidity conditions. After all, the internal volume of the glass-epoxy insulator is always dry, whereas the surface is the place where you can easily get a leakage problem due to dirt or moisture. That's where you have to prevent the leakage. Of course, crosstalk and high-frequency coupling problems are caused by adjacent foil locations and are cured by the same guarding and shielding just discussed to prevent foil leakages. To help you plan a good layout, think about what dv/dt and di/dt will do in a poor layout.

The field of pc-board layout is a subject unto itself. But there are some things you can do or add to a layout that will make testing the circuit much easier. Thoughtful designers have a store of these tricks, but I bet very few write them down. In my world, the unwritten rules are the ones that are broken, so we are trying to write them down. I recommend that all designers write down a list of their good ideas. Some layout tips from my list are

- Make sure that the signals you need access to for troubleshooting or analysis are easy to find and probe. Make a hole in the solder mask for accessibility.
- Include a silkscreen layer of labels in your layout artwork showing each component and its reference designation. It's also a good idea to label numbered test nodes and the correct polarity of diodes and electrolytic capacitors.
- Arrange the signal paths so that if you are desperate, you can easily break a link and open a loop, be it analog or digital.
- Many modern pc boards have multiple layers and sophisticated patterns of ground planes, power-supply buses, and signal flows. Troubleshooting such a board requires specialized techniques and skills and all sorts of "maps," so you don't get lost or confused. Make an effort to be sure that all the board's nodes are accessible, not hidden or buried on an inside layer.
- When possible, leave adequate space around components, especially ones that are more likely to fail and need to be replaced. Such components might be part of circuits that lead off the board and into the realm of ESD transients and lightning bolts and, thus, might occasionally fail.
- Locate delicate components away from the edge of boards, where they might be damaged by rough handling.
- Be careful using eyelets to connect different layers of foil on your pc board.

Years ago, plated-through holes were considered risky, so we used eyelets to connect the top and bottom foils. When these eyelets went through temperature cycling, the thermal stresses would cause the eyelets to lift the foil right off the boards. Even in the last year, I have seen advertisements that sing out the praises of eyelets on pc boards, so be careful when using them. These days, plated-through holes are quite reliable, but I still like to use them in conjunction with eyelets when I have enough room. It just makes me feel more comfortable.

More important than these layout conveniences is

You can ease the testing of your circuit by including such items as test points and labels in your layout.

that your layout not interfere with and, if possible, enhance the expected performance of the circuit. Most designers of digital circuits are aware that with high-speed logic, you can't just run the fast signals any old way. You have to treat these signal paths as transmission lines and route them carefully. So, whether with printed-circuit foils or wire-wrapped conductors, most designers have learned to build digital circuits that work well.

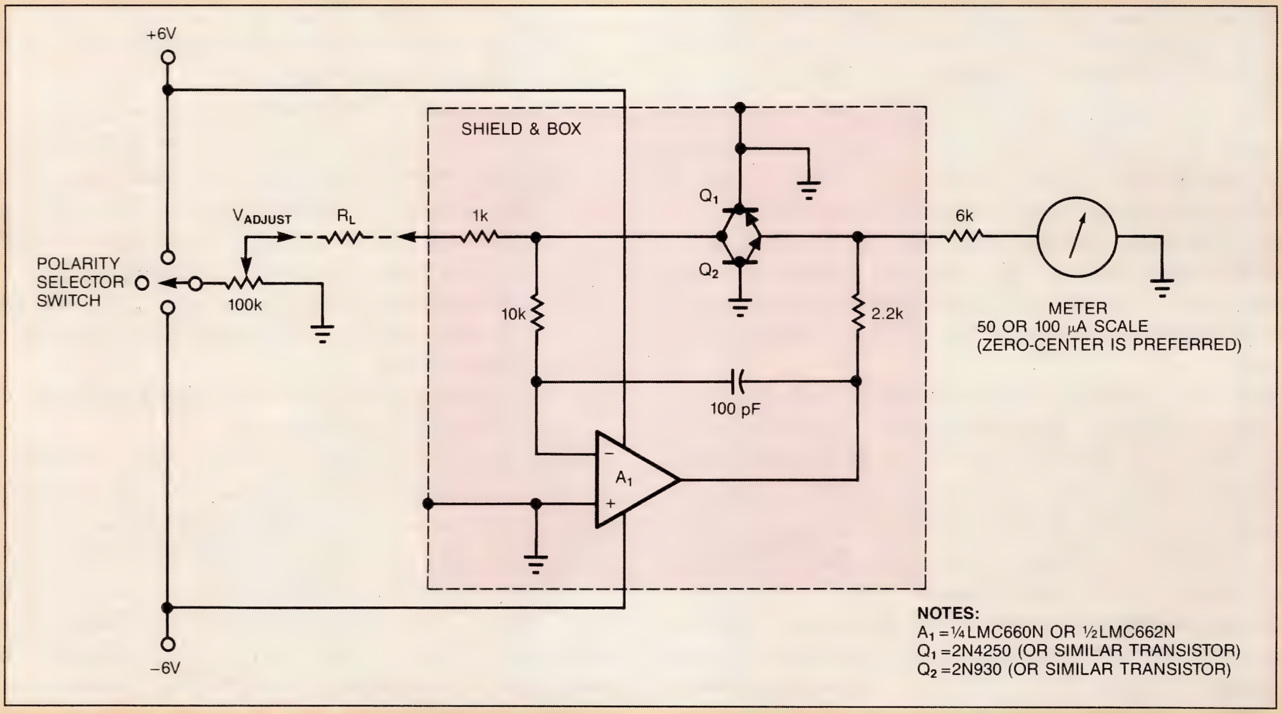
However, I have seen cases in which a wise digital designer had to add a few linear circuits to one corner of a mostly digital pc board. If the designer makes bad guesses about how to wire an op amp, the linear circuits may oscillate or work poorly. And, the availability of wire-wrap connections makes it tempting for the board designer to make a neat-looking layout with all the op amps and comparators and feedback resistors and capacitors in neat rows. Unfortunately, this neatness causes some critical interconnections to be a couple of inches apart. And then the designer is puzzled

Looking for leakages

When you have a leaky board or a slightly less-than-infinite-impedance connector or insulator, how do you test for leakage? There are basically two ways to measure leakage current.

The approach I have used for many years is to connect a couple of transistors as a wide-range, logarithmic, current-to-voltage detector across the feedback path of a low-bias-current op amp. These days, I'm not using vacuum tubes—I have graduated to an LMC660, as shown in the circuit of **Fig A.** I calibrated the meter with a hand-drawn scale to sense currents ranging from 1 pA to 1 mA and −1 pA to −1 mA **(Fig B).** As long as the air conditioning doesn't break down, I know my calibration won't drift much more than 10 or 20%, which is adequate to tell me which decade of current I am working in.

It's true that the DVM approach shown in **Fig C** has a little more accuracy and perhaps more resolution; but it is easily fooled by noise, and the digital readout doesn't show trends well. And, if you want to cover a wide range of currents, you have to plug in



NOTES:
A_1 = ¼LMC660N OR ½LMC662N
Q_1 = 2N4250 (OR SIMILAR TRANSISTOR)
Q_2 = 2N930 (OR SIMILAR TRANSISTOR)

Fig A—You can use this circuit to test your board for leakage current. *The transistors are connected across the op amp's feedback path in such a way that they act like a current-to-voltage detector.*

as to why the amplifiers and comparators are oscillating so badly.

So, pc-board designers should be made aware that the layout of linear ICs can be quite critical. The 2-in. spacing that you would never allow, for example, between a digital IC and its bypass capacitor is the same 2-in. spacing that makes an op amp unhappy when its inverting or noninverting input has to travel that distance to various resistors. As I will explain in future articles on active-circuit troubleshooting, there are good reasons to keep those summing-point foils short, neat, and compact.

Engineers often assume that a printed-circuit trace has virtually no resistance and no IR drop. But, when you run large currents through a foil run, you will be unpleasantly surprised by the IR drop you'll see. The classic example is a layout where the signal ground for a preamplifier is mixed and shared with the ground return path for the power supply's bridge and filter capacitor. This return path will see ampere-size surges

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different resistors or wait for the DVM to autorange, which is not my idea of fun. On the other hand, you can find a DVM almost anywhere, so this approach is easy to implement.

Whichever detector you use, apply a reasonable voltage across the unknown impedance and see where the leakage gets interesting. This method can also be used for diodes and transistor junctions. The op-amp circuit is not recommended for measuring the leakage of large-value capacitors. Neither is the DMV approach because of the slow charging of the large capacitance and soakage, or dielectric absorption, effects. But, if you're desperate and start out with a low value of R_{sense}, you can eventually get some approximate measurements.

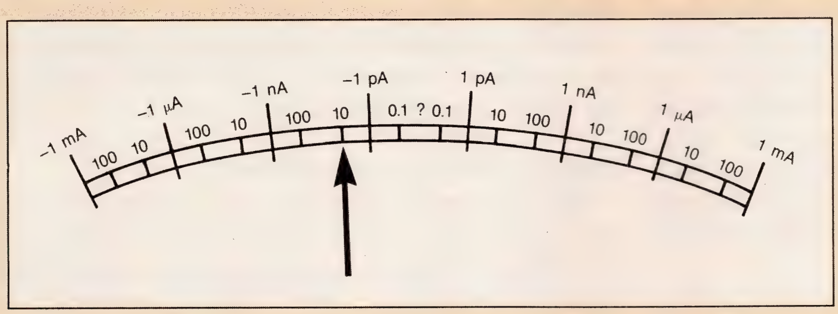
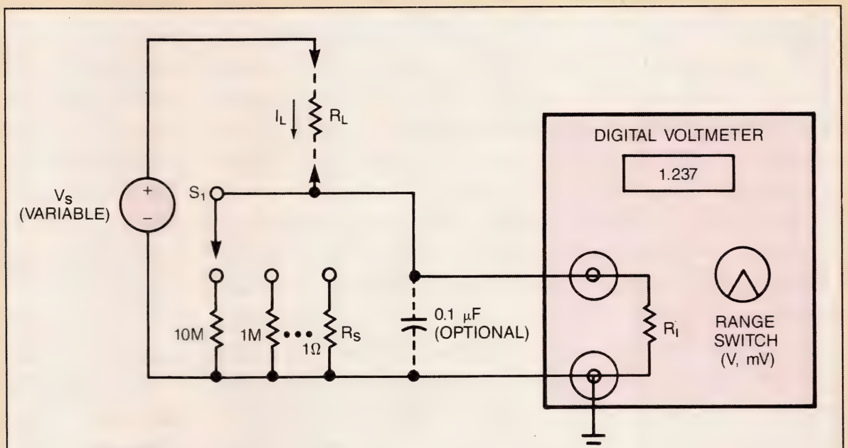


***Fig B—You can calibrate the logarithmic-current-meter** circuit of **Fig A** to sense currents between −1 mA and −1 pA and between 1 pA and 1 mA.*



NOTES:
S_1 =RESISTOR SENSE SELECTOR
R_I =DVM INPUT IMPEDANCE. FOR SOME DVMs, R_I IS 10M IN SOME RANGES (CONSULT USER'S MANUAL)

***Fig C—The DVM approach is an alternative** to the approach illustrated in **Fig A** for testing leakage. You can calculate the leakage current from Ohm's Law: $V_S = I_L \times R_S$, or $I_L = V_S/R_S$.*

Leakage troubles usually start after the board has been soldered or washed with a contaminated solvent.

120 times per second. Needless to say, the preamplifier won't have "low noise" until the path for the current surges is essentially divorced from the preamp's ground. For precision work, your pc-board layout must include well-thought-out ground paths for your sensitive circuitry.

When you think about it, separating power-supply grounds that carry lots of current from voltage-sensing circuitry is similar to Kelvin connections, which are commonly used in test instruments. A Kelvin connection uses four wires: one pair of leads is meant to carry current and the other pair senses voltage across a device. Keeping the idea of Kelvin connections in mind when designing your pc board will help you optimize your grounding scheme.

Avoid cold-soldered joints

I have a few comments to add about solder; most of the time we take it for granted. You'll normally use ordinary rosin-core tin-lead solder. If you avoid jiggling the soldered joint as it is cooling, you won't get a cold-soldered joint. But you should know what a cold-soldered joint looks like and how much trouble one can cause in a critical circuit. I feel sort of sad that today's young people aren't building kits for electronic equipment. In the old days, you could learn all about cold-soldered joints before you got into industry. But with modern wave-soldering equipment, it's fairly easy to avoid cold-soldered joints.

If for some reason you have acid-core solder around—it's mainly used for plumbing and is not found in most electronics labs, for good reason—keep it strictly segregated from ordinary rosin-core solder. Acid will badly corrode conductors. Also, keep specialty solders such as high-temperature solder, low-temperature solder, silver solder, and aluminum solder in a separate place to avoid confusion.

Printed-circuit boards aren't the only assembled component you'll have to contend with while trying to make circuits work. In Tracy Kidder's Pulitzer Prize-winning book, *The Soul of a New Machine* (**Ref 1**), one of the crucial moments occurs when the engineers explain to a management team that their new computer has a flaw that occurs only rarely but is driving them to distraction. One of the managers stands thoughtfully for a while and then reaches over and warps the main board: Scrunch, scrunch. To the horror of the project engineers, the scrunching correlates with the terrible intermittent problem. When the main board's DIP sockets were replaced, the problem disappeared.

Like a faithful dog, a connector is expected to do its job without question, and it usually does. However, on the rare occasion when one does go bad, the connector usually becomes intermittent before it fails utterly. Fortunately, many engineers and technicians learn early on that the way to check an intermittent problem is to make it reveal itself when the board's connector is plugged in and out while the power is on.

But don't all the instruction books say that you shouldn't plug in the board with the power on? Sure. But I've never gotten into more trouble plugging a board into a hot connector than the trouble I've gotten out of. There may be some boards that are destroyed or damaged by this method, but they are in the distinct minority and should be studied. One way to help avoid problems is to make the ground fingers on a printed-circuit edge connector stick out longer than the other fingers. Thus, ground will be established before any other connection. Still, if you have a board that tends to latch up because the power-supply sequencing may be improper, you have to be prepared to stop plugging the board into that hot socket—fast.

Learn by fiddling and tweaking

There are many situations that can foul things up, but we all tend to learn more from fiddling around with things, tweaking and unplugging, than by purely cerebral processes. Once I had a technician who thought that DIP sockets should not be secured in place by tack soldering but by glue. This technique worked fine for a while, but occasionally the sockets would act like an open circuit on one pin or another. To solve the problem, we used an old technique. We traced the circuit coming into the IC, and it was fine. We traced the signal coming out of the IC; nothing. Then, we traced the signals on the pins of the DIP itself; the signals were not the same at all. I finally realized that the glue was getting into the internal voids of the socket and preventing the IC's pin from making a true connection.

We banned the glue from that task, and the problem went away, mostly. Still, both before and after that time, we have seen sockets that just failed to connect to an IC's pin. You merely have to probe to the pin of the IC itself, not just to the socket, to nail down this possibility. Sometimes, the pin goes into the socket and actually fails to connect; but, more often than not,

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the pin is simply bent under the package.

There is one other kind of problem you can have with a socket, as a friend of mine recounted. He was trying to troubleshoot a very basic op-amp circuit whose waveforms did not make sense. After several minutes, he turned his circuit over and realized he had forgotten to plug an op amp into the socket. This example leads us to McKenna's Law, named after an old friend of mine: "You can't see it if you don't look at it." We invoke this law when we discover that we forgot to plug in a line cord or connect something. A vital part of troubleshooting is realizing that we are all at the mercy of McKenna's Law when we get absent-minded.

Connectors and sockets usually do more good than harm. They permit you to check options and perform experiments that may seem absurd and preposterous, yet are instructional and life-saving. Once a friend was in the throes of a knockdown-dragout struggle to troubleshoot a fast A/D converter. He had tried many experiments, but a speed problem eluded him. He asked me if he should try a socket for a critical high-speed component. At first, I was aghast. But, after I thought about it and realized that the socket would add barely 1 pF of capacitance, I said, "Well, OK, it may not do much harm."

The addition of the socket led to the realization that the speed problem was critically correlated with that component, and the problem was soon solved. The socket that might have caused terrible strays actually caused almost no harm and, in fact, facilitated the real troubleshooting process. If nothing you do leads in an encouraging direction and you have a half-baked notion to tell your technician to install a socket, that may be the best idea you have all day. The socket may do very little harm and could lead to many experiments, which might give you the vital clue that puts you on the track of the real culprit.

Now, I'll add a few pithy comments about wire and cable. Not all wire is the same. For example, when I first got a job in electronics, I was having a lot of trouble with Teflon-insulated wire. The wires would often break right at the point where the solder stopped. After several engineers assured me that all wire was the same and suggested that I was just imagining things, I was ready to scream.

Finally, I found an engineer who admitted that cable manufacturers couldn't put individually tinned wires into a Teflon insulator, as they do with plastic-insulated wire. At the temperatures at which the Teflon is extruded, the solder would all flow together, thus making the stranded wire a solid wire. Instead, cable manufacturers use silver-plated wire strands for Teflon-insulated wire. With this type of wire, solder tends to wick up into the strands, thus making the wire quite brittle. Once I understood the wire's structure, I was able to solve my problems by adding strain relief for any bends or pulling stresses.

Whether you are designing a pc board or an IC, *your circuit's layout is critical to its performance. For certain designs, you'll need to carefully consider the placement of each component, as Pease and his group demonstrate.*

As I mentioned in the section on equipment for troubleshooting, the ordinary plastic-insulated single-conductor wire that is used in telephones has just the right stiffness to make good twisted-pair wire for making capacitors with values of 1, 2, or 5 pF. The wire doesn't have a Teflon dielectric, but it's good enough for most applications.

Consider your wire type

Shielded or coaxial cables, such as RG58U, RG174, shielded twisted pairs, and other special flat cables, all have their place in the job of getting signals from here to there without undue attenuation or crosstalk. When you have a large number of wires mindlessly bundled together and you don't have any bad crosstalk, you're witnessing a miracle. Often you have to unbundle the wires and separate the offending ones or the sensitive, delicate signals from the rest. Also, you may end up rewiring some or all of the wires into shielded cables.

Remember, Teflon is a good insulator, but air is even better. If you have to add struts, standoffs, or spacers to make sure that the critical wires stay put, go right ahead. If you have problems, the wire manufacturers can give you some advice.

Conversely, just as you use Teflon or air when you need a superior insulator, you have to be careful to get your best conductances. A friend who is an amateur radio operator says that many kinds of problems in RF circuits arise because nuts and bolts are used to make ground connections. If a lock washer or star washer is not included, the mechanical connection can loosen, the ground impedances will change with every

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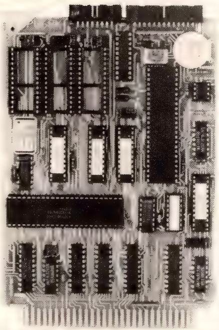

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little stress or strain, and nasty intermittent electrical problems will result. So, a major factor in the reliability of these circuits is ensuring the integrity of all bolted joints by always including star washers. And, make sure that wires and connectors do not get so loose as to hurt the reliability of your circuit or system.

When you use shielded cable, should you ground the shield at one end or at both ends? Many cases call for a ground at the receiving end of the cable, but there are cases in which the shield is the main ground return. Neither way is necessarily bad, but be consistent. Likewise, in the design and the execution of the design, avoid ground loops, which can cause weird noise problems. In my systems, I build my analog ground system completely separate from the digital ground and make sure that the case or package ground is also strictly divorced. Then, I add one link from the analog ground to the digital ground and another link to the case or chassis. This technique works well for me, and I recommend it.

It is a little-known fact that some coaxial cable can degrade just sitting on the shelf. Types whose codes end in "U," such as "RG-58U," have an "uncontaminating" outside shield. In contrast, RG-58 might have an outside shield with superior physical characteristics, but it could, over time, degrade the electrical properties of the cable—specifically, its UHF attenuation. So, even in something as simple as a wire, there may be more problems than meet the eye. **EDN**

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Acknowledgments

The author wishes to thank Cindy Lewis of Sun Circuits Inc (Santa Clara, CA) for her help in preparing the table. Bob also wants to thank the 40-odd friends who helped review the drafts of these articles, correct his mistakes, and suggest additions. Special thanks to Jim Moyer, Tim Regan, Dennis Monticelli, and Dan Strassberg. Credit goes to Mineo Yamatake for his elegant thermocouple amplifier design, to Steve Allen for his photography, to Erroll Dietz as key grip, to Carlos Huerta as gaffer, and to Joyce Gilbert for all her typing.

Author's biography

*For information about Bob Pease, see the **box,** "Who is Bob Pease, anyway?" in the January 5, 1988, edition of EDN.*

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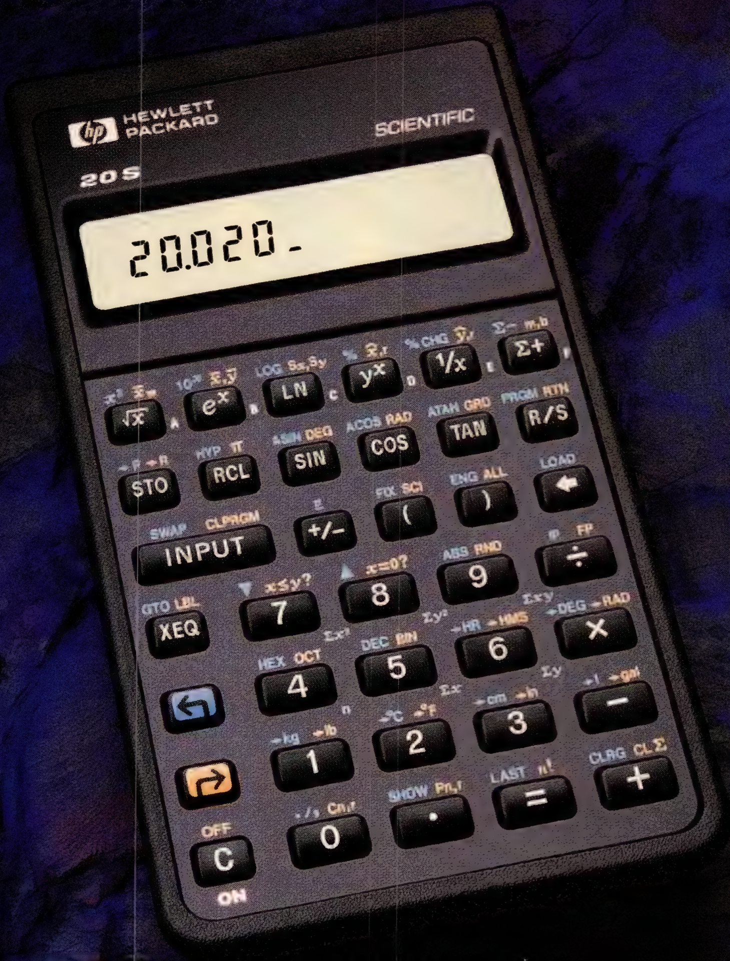

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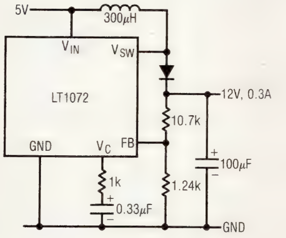

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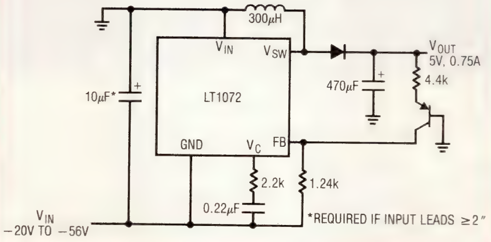

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CIRCLE NO 81

PLD implements programmable delay

Steven M Chew
Fairchild Weston Systems, Syosset, NY

Using an 8-bit up/down counter and one PLD (**Fig 1**), you can delay input signals from 1 to 32 clock cycles, depending on the value you set up in S_1.

As Ready In goes from low to high, the PLD enables the counter to count up from zero. As the counter counts, the PLD compares the counter's output to the preset number. When the two numbers match, the PLD disables counting and sets Ready Out high. As long as Ready In remains high, the circuit does nothing. When it goes low, the PLD enables the counter to count down. When the counter reaches zero, its RCO (pin 13) goes active low, and the PLD forces Ready Out to a low. The pulse to be delayed must be longer than the delay itself.

The PLD used in this design is the MMI PAL16L8 (see **Listing 1** for equations), but any other that can provide enough product terms will work. The delay is limited to 32 clocks cycles because the circuit uses only five counter-output bits. If you need larger delays, use a larger PLD or two PLDs. Using an MMI PAL16L8B-2, this circuit functions at a clock speed of 10 MHz.

LISTING 1— EQUATIONS FOR DELAY-CIRCUIT PLD

```
/CO = A0 * /B0 + /A0 * B0
      A1 * /B1 + /A1 * B1
      A2 * /B2 + /A2 * B2
      A3 * /B3

/S1 = CO * A3 * /A4 * /B4 +
      CO * A3 * A4 * B4 +
      CO * /B3 * /A4 * /B4 +
      CO * /B3 * A4 * B4 +
      /IN

/EN = IN * /OU + /IN * OU

/RS = T * OU + C1 * OU

/OU = /CO * RS +
      /A3 * B3 * RS +
      A4 * /B4 * RS +
      /A4 * B4 * RS +
      C1 * RS
```

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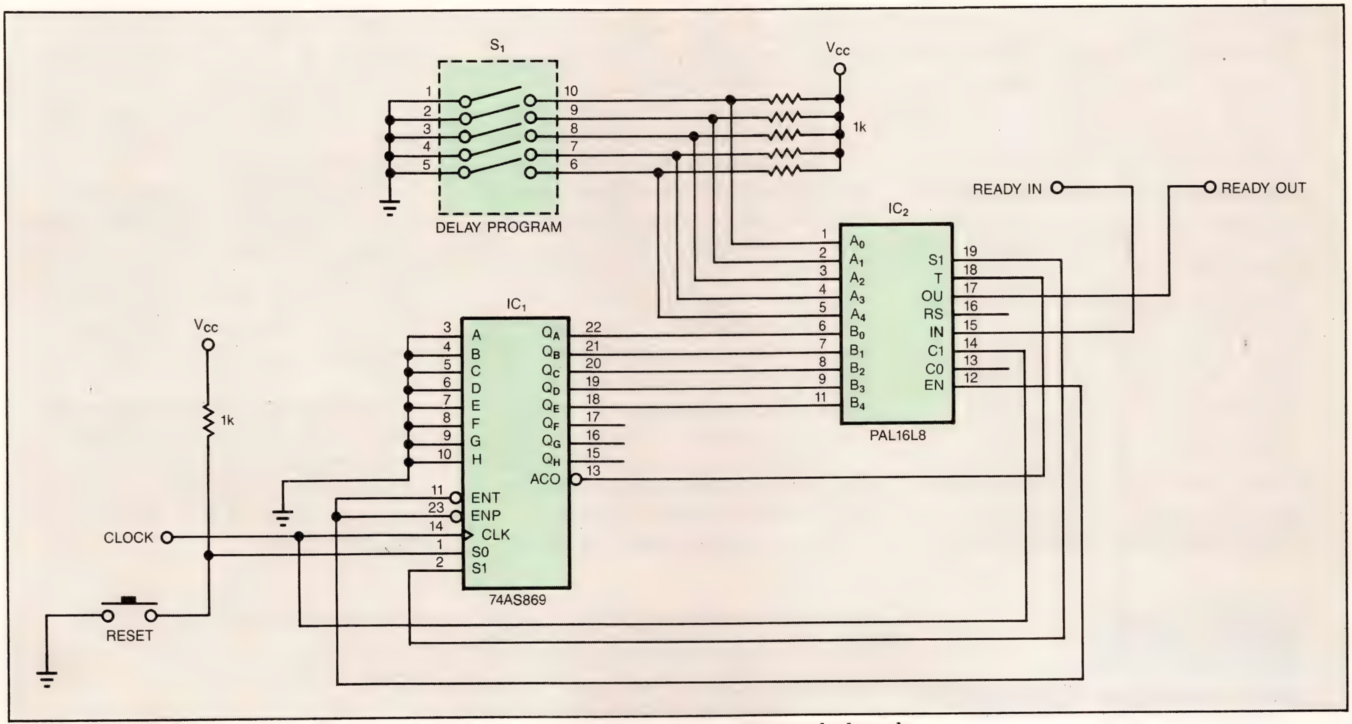

*Fig 1—**By using two ICs and a DIP switch,** you can delay Ready In by up to 32 clock cycles.*

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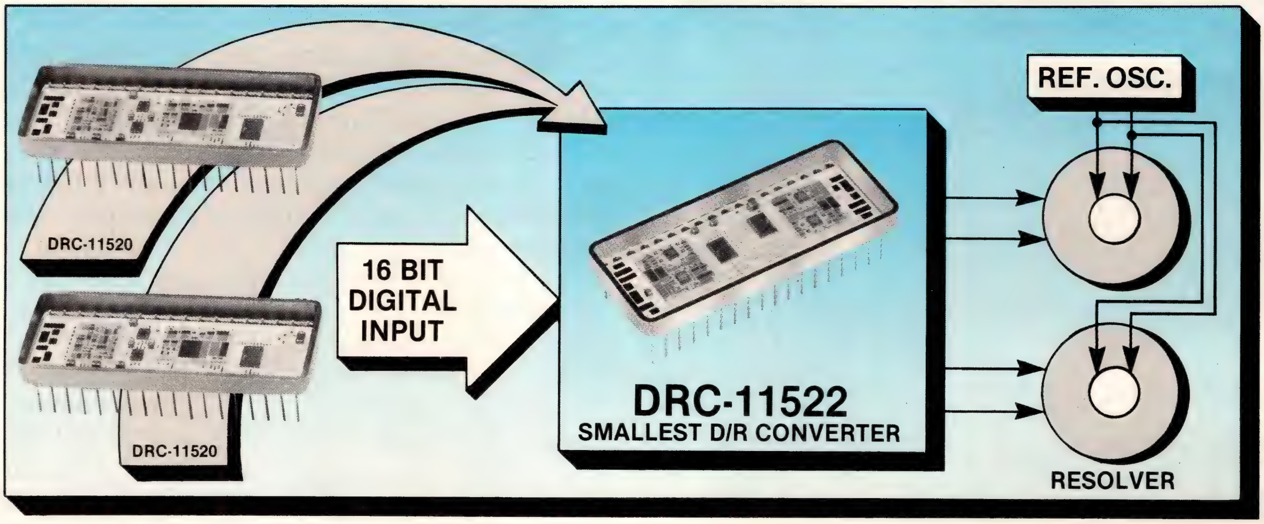

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Each of the 2 channels of the DRC-11522 provides outputs which are the product of the reference input and the sine and cosine of the digital input angle. Since the reference input may be an arbitrary waveform, the unit may be used in a number of useful applications. With a resolver reference, a digital-to-resolver converter is implemented; with a DC reference, a digital-to-sin/cos DC converter is implemented; and with a sawtooth reference, a PPI display sweep generator is implemented.

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Create universal logic with wired-OR ECL

John Hall and Joe Swanzy
Summation Inc, Kirkland, WA

By taking advantage of the open-emitter characteristic of ECL, you can wire-OR signals to create a fast circuit with an almost universal Boolean relationship between the two inputs. In **Fig 1,** an OR gate superimposed on the connection of two paths represents a wire-ORed connection.

Table 1 shows the Boolean combinations you can achieve with this circuit depending on the state of the five latched control signals: QUAL_OR_H, Q0_REQ, Q0_MASK, Q1_REQ, and Q1_MASK. The Q1_MASK and Q0_MASK controls enable the two inputs. The Q1_REQ and Q0_REQ controls determine whether the inputs are inverting or noninverting. And the QUAL_OR signal determines whether the relationship between the inputs is OR or AND.

To Vote For This Design, Circle No 748

TABLE 1—BOOLEAN COMBINATION TRUTH TABLE

	CONTROLS				
OUTPUT	QUAL_OR_H	Q0_REQ	Q0_MASK	Q1_REQ	Q1_MASK
Q0	1	1	0	1	1
NOT Q0	1	0	0	1	1
Q1	1	1	1	1	0
NOT Q1	1	1	1	0	0
Q0 AND Q1	1	1	0	1	0
Q0 AND NOT Q1	1	1	0	0	0
NOT Q0 AND Q1	1	0	0	1	0
NOT Q0 AND NOT Q1	1	0	0	0	0
Q0 OR Q1	0	0	0	0	0
Q0 OR NOT Q1	0	0	0	1	0
NOT Q0 OR Q1	0	1	0	0	0
NOT Q0 OR NOT Q1	0	1	0	1	0
ALWAYS 1	1	1	1	1	1
ALWAYS 0	0	1	1	1	1

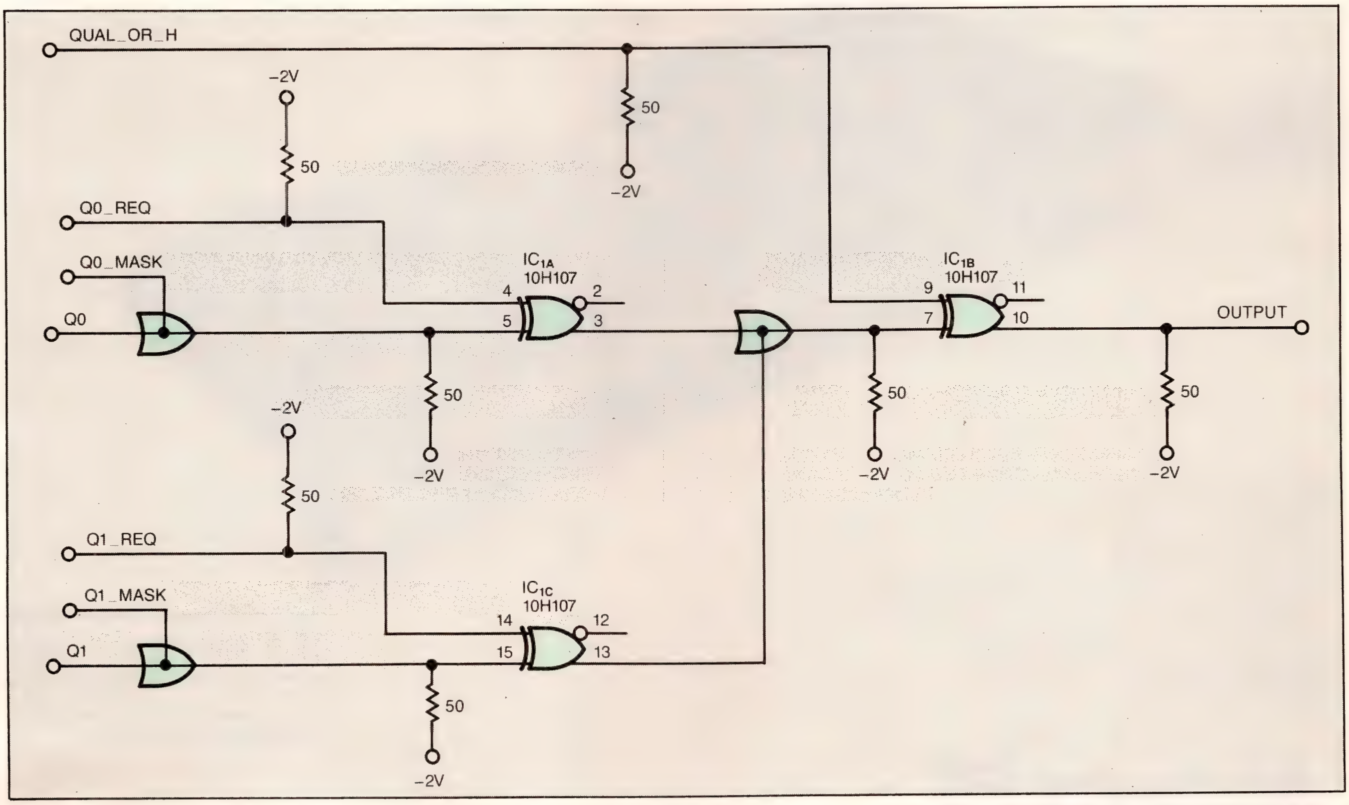

***Fig 1—You can use this ECL circuit to achieve** an almost universal Boolean combination of two inputs. The propagation delay is 5 nsec max.*

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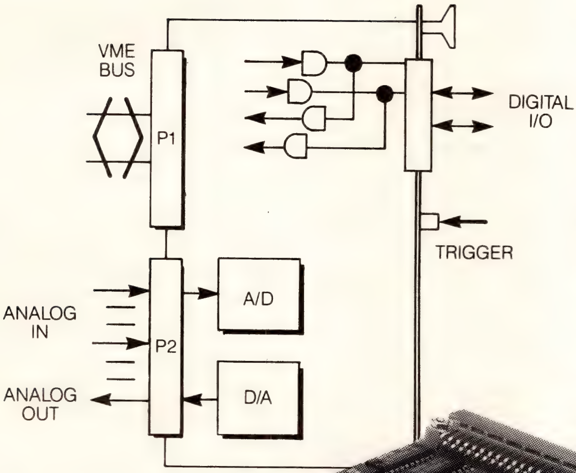

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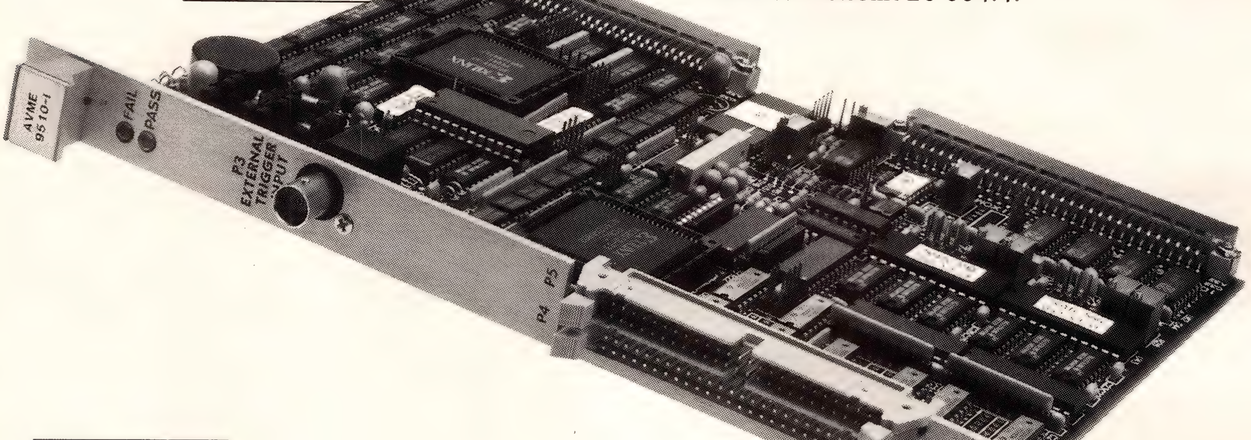

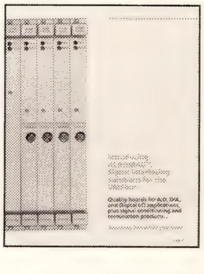

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CIRCLE NO 82

Circuit bounds output frequency

Christopher R Paul
Coherent Communications, Hauppauge, NY

You can drive the circuit shown in **Fig 1** with a periodic waveform, and the circuit will pass that signal unaffected if its frequency is in the F_{MIN}-to-F_{MAX} range. If F_{IN} lies outside this range, F_{OUT} will be held at either the upper or lower limit. You can then use F_{OUT} to drive a 74HC4046 type 1 phase detector, for example, and guarantee that the PLL won't lock to the wrong multiple of its input reference frequency.

IC_{1A} and IC_{1B} limit the circuit's maximum output frequency. If the frequency of F_{IN} is less than that of F_{MAX}, IC_{1A} will be clocked at least once between every pair of IC_{1B} clocks. The Q output of IC_{1A} will be updated to hold the value of IC_{1B}'s $\overline{Q}$ in time for the next $2F_{IN}$ clock pulse. IC_{1B} will then toggle on every $2F_{IN}$ clock pulse, and its Q output will toggle at a frequency of F_{IN}.

If the frequency of F_{IN} exceeds that of F_{MAX}, IC_{1B} will not toggle on every $2F_{IN}$ clock pulse. However, IC_{1A} will toggle for every $2F_{MAX}$ clock, so that IC_{1A}'s Q output toggles at a rate of F_{MAX}. Since there is at least one $2F_{IN}$ clock for every IC_{1A} toggle, IC_{1B} will pass every transition of IC_{1A}. Thus, the frequency of IC_{1B}'s output will be limited to F_{MAX}. The part of the circuit consisting of IC_1 completely determines the frequency of F_{OUT} in all cases where F_{IN} is greater than F_{MIN}. Under these conditions, pin 1 of IC_{4A} never changes state.

When F_{IN} falls below F_{MIN}, extra transitions are generated by IC_2, IC_3, IC_{4B} and IC_{4C}. These transitions appear at the $\overline{Q}$ output of IC_{3A} and add to the transitions of IC_{1B} to force a minimum frequency of F_{MIN} to appear at the circuit output.

The circuit may cause a 180° phase inversion between F_{IN} and F_{OUT}. This inversion is not a problem if the input comes from a VCO because the phase of the VCO is already ambiguous: At this point in a PLL circuit, the VCO isn't locked to the PLL in any particular phase relationship. **EDN**

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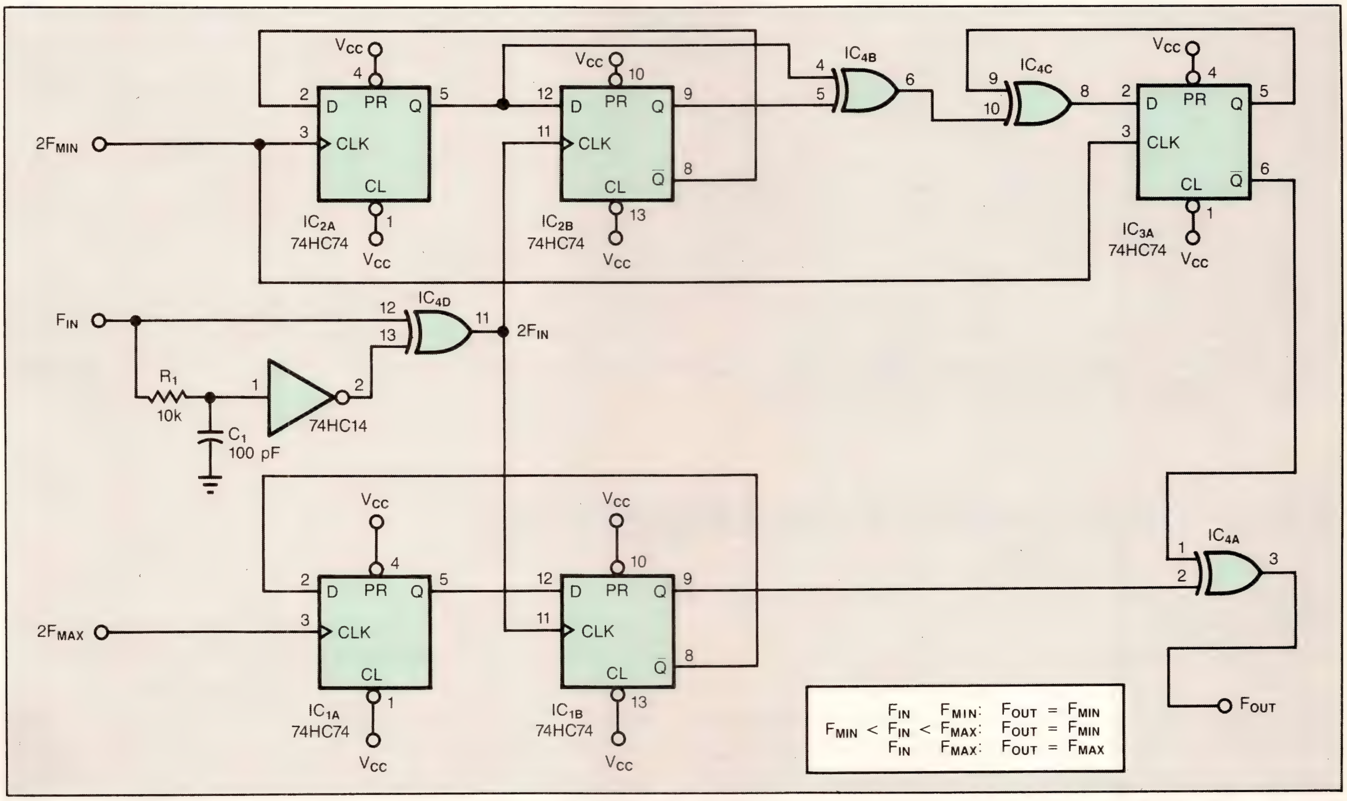

*Fig 1—**Designed to work with periodic waveforms such as VCO outputs,** this circuit constrains the frequency of F_{OUT} to be within the limits set by the signals F_{MIN} and F_{MAX}.*

MOSFET switch compensates sampler

Michael A Wyatt
SSAvD Honeywell, Clearwater, FL

You can reduce high-speed S/H voltage-offset errors in a simple FET and hold-capacitor design, by using a second MOSFET switch and gate as shown in **Fig 1.** The second MOSFET, Q_2, typically reduces offset by a factor of 10; but, with selected FETs, the offset was reduced from 43 mV to 2 mV—a 20-fold reduction.

Without the presence of the compensation network comprising Q_2 and IC_B, charge injection would cause voltage-offset errors. Q_1's gate-to-channel capacitance couples the gate of Q_1 to the hold capacitor, C_1. When you switch Q_1's gate from a 1 to a 0 to hold a sample, the portion of Q_1's gate voltage coupled to the capacitor alters the charge on C_1, which, in turn, causes a sample error.

The presence of Q_2 cancels the amount of charge coupled to C_1. As Q_1's gate voltage falls, Q_2's gate voltage increases, which produces a charge coupling to C_1 opposite to that caused by Q_1. Since Q_1 and Q_2 see almost the same voltage levels at their respective drain and source terminals during the sample-to-hold transition, their nonlinear capacitance vs voltage characteristics will tend to track and cancel.

You must drive the high-speed sampler shown in **Fig 1** from a low-impedance source or a high-speed buffer. Connect the output to a high-impedance load or buffer it with a high-impedance buffer as in **Fig 1**. The sampler can handle input signals of ±1V peak. **EDN**

To Vote For This Design, Circle No 746

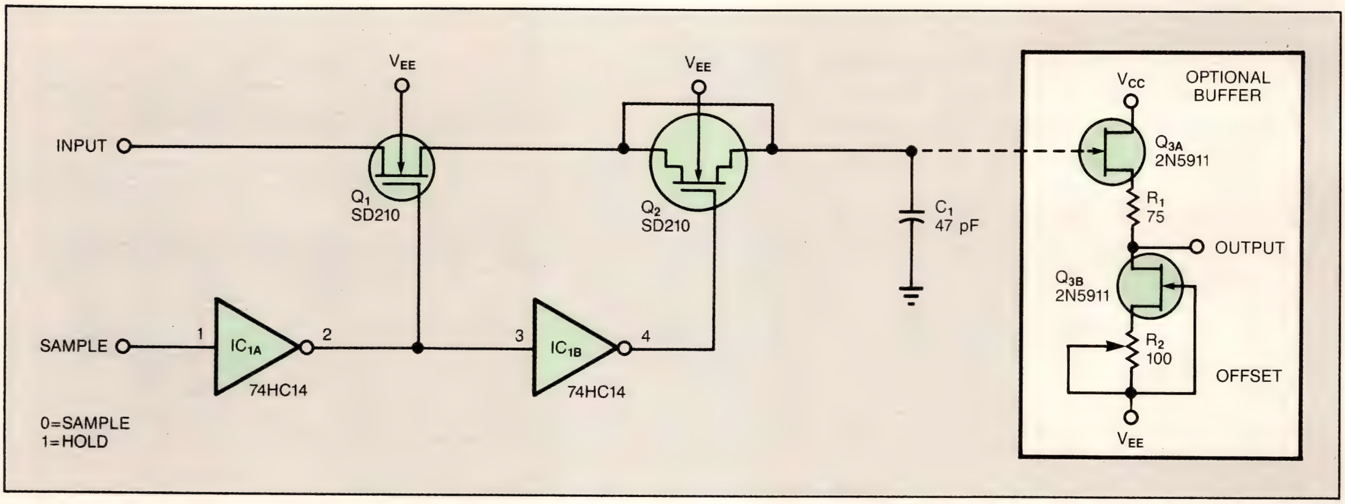

Fig 1—Adding a second switch, Q_2, and a second inverter, IC_{1B}, *to this high-speed sampler reduces the amount of charge-injection errors; Q_1 and Q_2's charge coupling effects are equal and opposite.*

One-shot avoids false triggering

Brady Barnes
Inter-Tel, Chandler, AZ

Most engineers are in agreement that one-shots are nothing but trouble. One-shots are prone to false triggering, and the pulse-width formula varies from manufacturer to manufacturer.

However, there are still times when one-shots are the best part for a design task. In these cases, you should consider using the circuit in **Fig 1**; it's more reliable and less prone to false triggering than the standard LS122 and LS123 parts. Also, the CMOS HC132 consumes less power than the LS parts and is packaged in a 14-pin DIP, compared with the 16-pin LS123.

The circuit as it stands in **Fig 1** triggers on only

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Internally the MAN amplifiers consist of two stages, including coupling capacitors. A designer's delight, with all components self-contained. Just connect to a dc supply voltage and you are ready to go.

The new MAN-amplifiers series…
another Mini-Circuits' price/performance breakthrough.

MODEL	FREQ. RANGE (MHz) f_L to f_u	GAIN dB min	GAIN dB flatness††	MAX. OUT/PWR† dBm	NF dB (typ)	DC PWR 12V, mA	PRICE $ ea. (10-24)
MAN-1	0.5-500	28	1.0	8	4.5	60	13.95
MAN-2	0.5-1000	19	1.5	7	6.0	85	15.95
MAN-1LN	0.5-500	28	1.0	8	2.8	60	15.95
◇MAN-1HLN	10-500	10	0.8	15	3.7	70	15.95
*MAN-1AD	5.500	16	0.5	6	7.2	85	24.95

††Midband $10f_L$ to $f_{u/2}$, ±0.5dB †IdB Gain Compression ◇Case Height 0.3 In.
Max input power (no damage) +15dBm; VSWR in/out 1.8:1 max.

*Active Directivity (difference between reverse and forward gain) 30 dB typ.

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CIRCLE NO 83

C118 REV. E

Design Entry Blank

$100 Cash Award for all entries selected by editors. An additional $100 Cash Award for the winning design of each issue, determined by vote of readers. Additional $1500 Cash Award for annual Grand Prize Design, selected among biweekly winners by vote of editors.

To: Design Ideas Editor, EDN Magazine
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ISSUE WINNER

The winning Design Idea for the November 24, 1988, issue is entitled "JFET doubles isolator's bandwidth," submitted by Steven C Hageman of Calex Manufacturing Co (Pleasant Hill, CA).

Your vote determines this issue's winner. All designs published win $100 cash. All issue winners receive an additional $100 and become eligible for the annual $1500 Grand Prize. **Vote now,** by circling the appropriate number on the reader inquiry card.

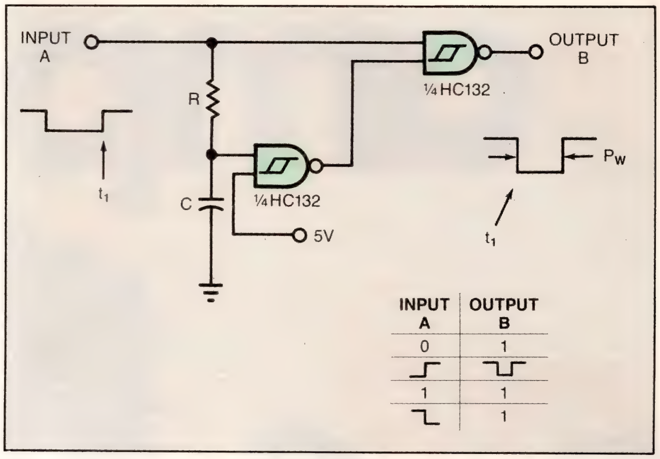

Fig 1—You can create your own reliable one-shot *using the 74HC132 NAND Schmitt trigger. The circuit as shown is positive-edge triggered and produces a low-level pulse.*

positive-going edges of the input signals and creates an active-low pulse of width P_W on the output, where

$$P_W = -RC\ln(1 - V_T^+/V_{A\text{-HIGH}}).$$

V_T^+ is the positive-going threshold voltage, and $V_{A\text{-HIGH}}$ is the "high" voltage level of the input signal. (Assume $V_{A\text{-LOW}} \approx 0V$ and $V_{A\text{-HIGH}} > V_T^+$.)

As with 74LS123s, the output pulse width can vary widely because of the tolerances of R and C and the possible ranges of $V_{A\text{-HIGH}}$ and V_T^+. If you power the circuit from a 5V supply, V_T^+ can range from 1.8 to 3.5V. If you estimate the range of $V_{A\text{-HIGH}}$ to be from 4.5 to 5V and your resistor and capacitor have 5 and 20% tolerances, respectively, then the pulse width could vary by a factor of 5.5. If this range seems excessive, it is no more so than that of an LS123.

To modify the circuit to trigger on negative edges of the input signal, simply use the remaining two gates in the HC132 package as inverters. Or, you can implement a dual one-shot by using the present circuit and all four gates in the HC132's package.

Note that this circuit only works when the pulse width of input A is wider than the time constant of the RC network. If A goes low before C charges up to the threshold voltage, then output B will simply go high again. So, your desired output pulse must be shorter than the input pulse in order to use this circuit. Because of this restriction, this circuit cannot function as a retriggerable one-shot.

Recommended ranges for R and C are 10 to 100 kΩ and 100 pF to 10 μF, respectively. These values of R and C yield typical pulse widths of 700 nsec to 700 msec—a range of six orders of magnitude. EDN

To Vote For This Design, Circle No 749

Z I L O G

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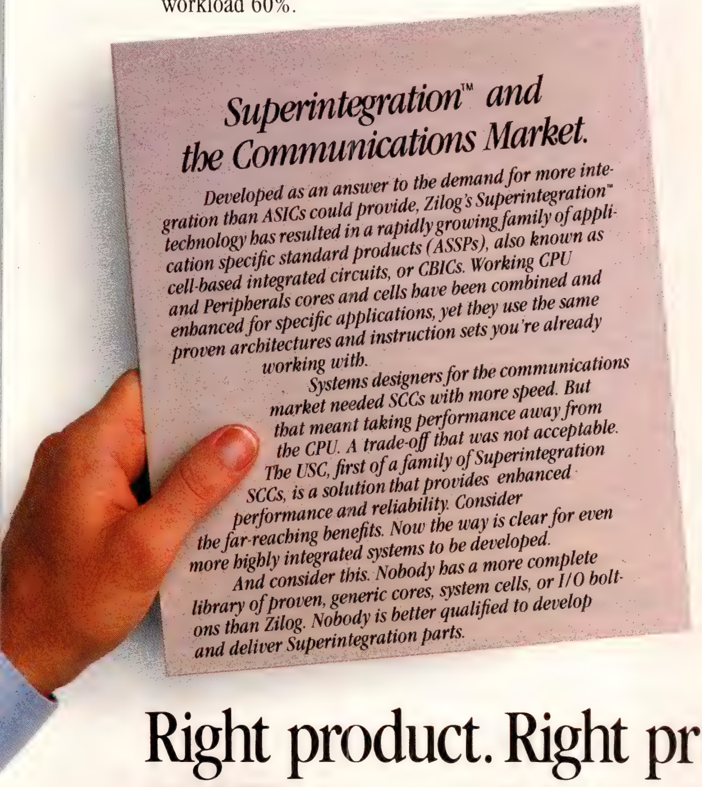

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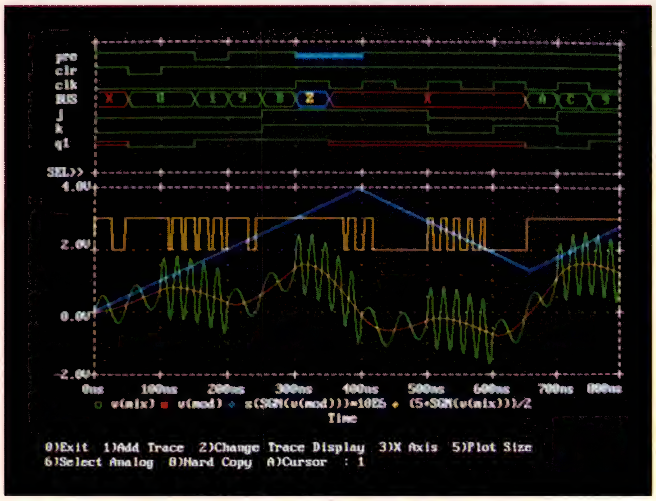
CIRCLE NO 84

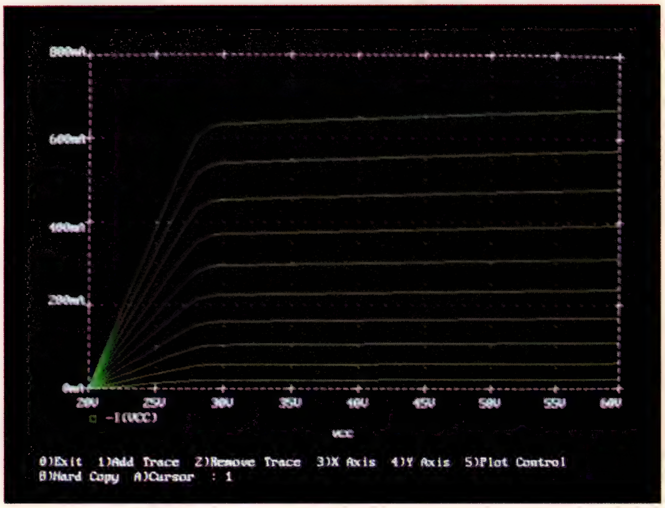
PSpice

Since its introduction five years ago, MicroSim's PSpice has sold more copies than all other Spice programs combined. Now PSpice 4.0 is available with the most significant new capabilities since the creation of PSpice in 1984.



Mixed Analog/Digital Simulation

With the Digital Simulation option, PSpice can simulate mixed analog and digital circuits. The option contains a 28-state, event-driven, logic simulation engine to efficiently process digital events. It is easy to use: analog and digital devices are included in the same netlist file, in the usual SPICE syntax, and may be freely interconnected. Probe, the graphics post-processor for PSpice, can display both analog and digital waveforms on the screen at the same time with a common time axis. PSpice includes a library of over 660 digital components.



Analog Behavioral Modeling

The Analog Behavioral Modeling option allows the user to describe a circuit block by giving the block's transfer function, either by formula or by table. Nonlinear transfer functions make it easy to model unique devices, such as Josephson junctions. Linear transfer functions are also available that describe the device in the frequency domain, either by a Laplace transform or by a frequency response table. Analog Behavioral Modeling helps top down design since a circuit block can be modeled by its transfer function at the beginning of a design and later replaced by the actual circuitry.

Extensive Device Libraries

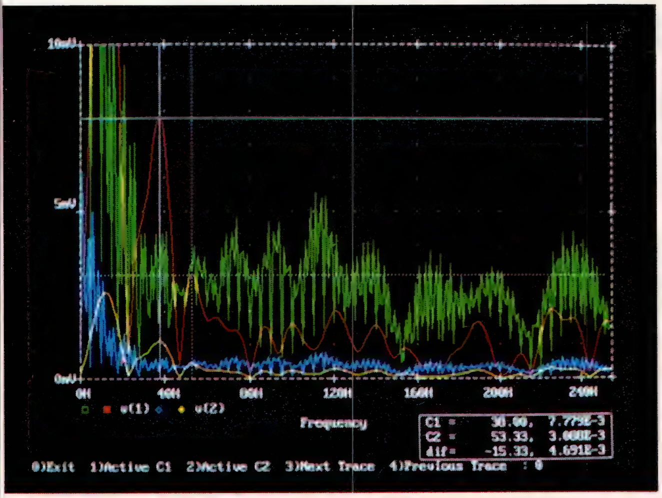
Included with each copy of PSpice 4.0 is an extensive library of over 2,200 analog components. The library files are not encrypted and may be modified by the

Extends the Bounds of Circuit Simulation

user. We also offer the Parts parameter extraction program to help you characterize additional devices.

Interactive Operation

On the PC, PSpice 4.0 allows interactive operation of the simulator. On-line help and pull-down menus assist one in using the simulator. An on-screen text editor which "knows" about the PSpice input format makes it easy to create or modify circuits, or use your favorite schematic editor.


10mV
5mV
0mV
0H
40H
80H
120H
160H
200H
240H
v(1)
v(2)
Frequency
0)Exit 1)Active C1 2)Active C2 3)Next Trace 4)Previous Trace : 0

```
C1 =     38.00,  7.773E-3
C2 =     53.33,  3.080E-3
dif=    -15.33,  4.691E-3
```

Enhancements and Options

In addition to the devices included in standard Spice, PSpice 4.0 includes these: GaAs MESFET's; BSIM MOS model; non-linear transformers, modeling saturation, hysteresis; and ideal switches for use with, for example, power supply and switched capacitor circuit designs. Extra options available: Monte Carlo analysis, including Sensitivity and Worst Case; Digital Files interface to popular logic simulators; and Device Equations source code for semiconductor devices.

Choice of Platforms

PSpice is available on these computers: the PC family, including the PS/2, under both DOS and OS/2; the Macintosh II, the Sun 3 and 4 workstations; and the VAX/VMS family, including the MicroVAX.

Technical Support

Each copy of PSpice comes with our extensive product support. Our technical staff has over 50 years of experience in CAD/CAE and our software is supported by the engineers who wrote it. With PSpice, expert assistance is only a phone call away.

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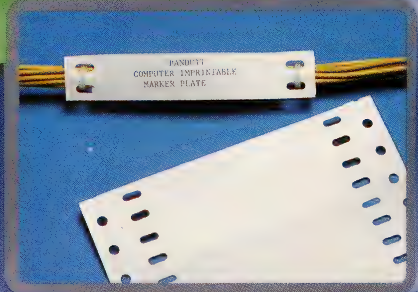

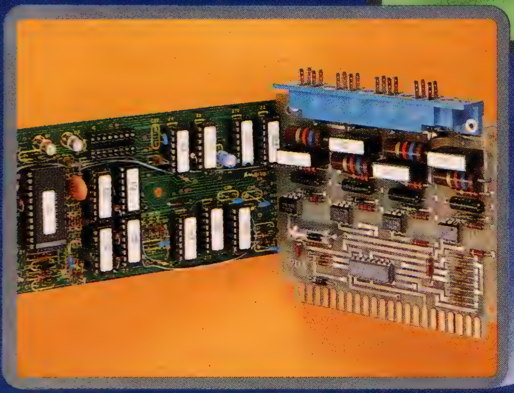

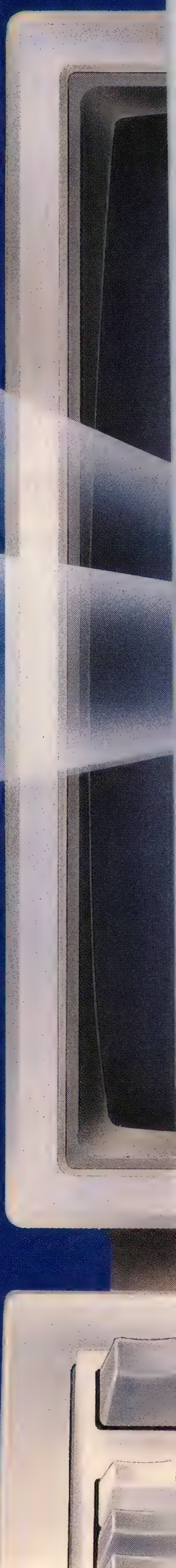

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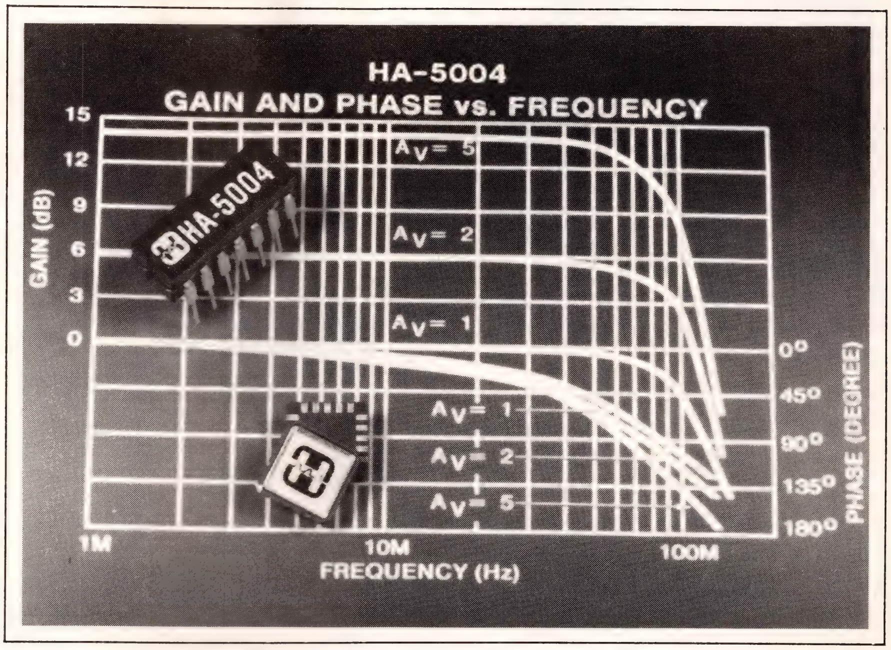


WIDEBAND AMPLIFIER

- *Has 100-MHz bandwidth*
- *Features current-mode feedback*

Optimized for low-gain applications, the HA-5004 wideband amplifier uses current-mode feedback to achieve higher closed-loop bandwidths than is normally possible with voltage-mode feedback. Unlike conventional amplifiers, the bandwidth and rise time of the HA-5004 are nearly independent of closed-loop gain. At a gain of 10, the amplifier's unity-gain bandwidth of 100 MHz reduces only to 65 MHz. The HA-5004 comes in two package configurations: a 14-pin ceramic DIP for commercial, industrial, and military termperature ranges, and an LCC package that is fully compliant with MIL-STD-883. Commercial ceramic DIP, $5.87; industrial ceramic DIP, $9.72; military ceramic DIP, $22.30; military LCC, $38.60 (100).

Harris Corp, Semiconductor Sector, Box 883, Melbourne, FL 32901. Phone (407) 724-7800.

Circle No 390

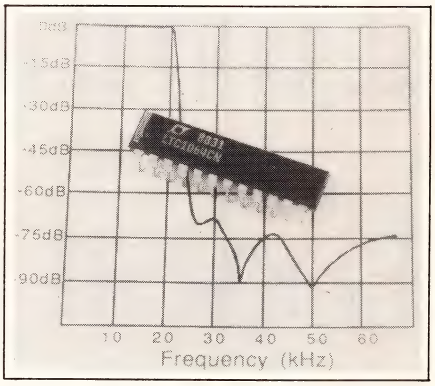
10-BIT A/D CONVERTER

- *Includes sample-and-hold circuit*
- *Needs only 900 mW of power*

The HA19214 10-bit A/D converter, which has a built-in sample-and-hold circuit, features a typical conversion rate of 20 million conversions/sec. This high rate is made possible by a 2-step parallel conversion method that simultaneously calculates the upper and lower five bits. The device has a typical signal-to-noise ratio of 52 dB at an input frequency of 5 MHz. The chip's digital output is high-speed-CMOS compatible, and the clock input can interface with CMOS and TTL logic. The chip operates from ±5V supplies, consumes only 900 mW of power, and comes in a 42-pin DIP that has 0.070-in. pin spacing. Sample price, $240.

Hitachi America Ltd, Semiconductor Div, 2210 O'Toole Ave, San Jose, CA 95131. Phone (408) 435-8300. TLX 171581

Circle No 391



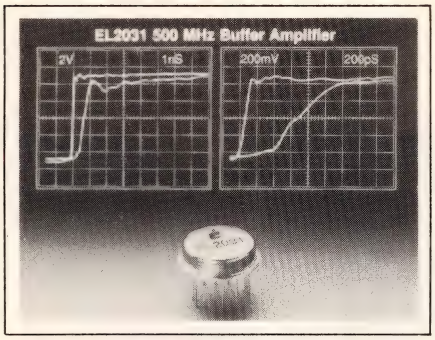
QUAD FILTER

- *Switched-capacitor type*
- *Implements 8th-order filters*

You can use the LTC1064 clock-tunable, quad, switched-capacitor filter to implement 8th-order Cauer, Butterworth, Bessel, Chebyshev, and other filters. With the LTC1064, an 8th-order Butterworth lowpass filter has a wideband noise of 80 μV rms, a corner frequency to 140 kHz, a total harmonic distortion of 0.015%, and an attenuation of −48 dB/octave. Using external resistors, you can configure each biquad filter section of the LTC1064. You use an external clock to program the center frequencies. For a Q of ≤8, the center-frequency range is 0.1 to 100 Hz; for a Q of ≤5, you can extend the center-frequency range to 140 kHz. The maximum clock frequency is 7 MHz, and the clock-to-center-frequency ratio for all four sections is either 50:1 or 100:1. 24-pin DIP; $8.40 (OEM qty).

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (800) 637-5545.

Circle No 392



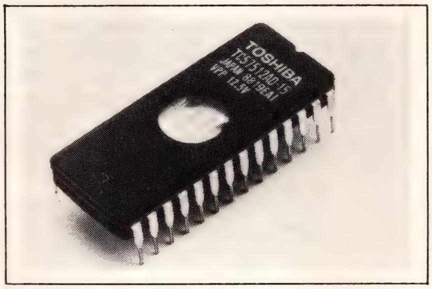
BUFFER AMPLIFIER

- *Features 8000V/μsec slew rate*
- *Has −3-dB bandwidth of 550 MHz*

Designed for use as a pin driver for automated test equipment and for digital-to-analog output buffering, the EL2031C features a slew rate of 8000V/μsec and a −3-dB bandwidth of 550 MHz into a 100Ω load. It has a minimum output swing of ±6.2V over the operating temperature range of 0 to 70°C with 100-mA peak load currents. The device includes internal bypass capacitors to minimize the effects of package leads and pc-board capacitances and inductances. 12-pin TO-8 package, $40 (100).

Elantec, 1996 Tarob Ct, Milpitas, CA 95035. Phone (408) 945-1323.

Circle No 393



CMOS EPROM

- *Available with either 150- or 200-nsec access times*
- *Has 64k-byte × 8-bit organization*

The TC57512AD-15/20 CMOS EPROM is electrically programmable and ultraviolet erasable. Power dissipation for the EPROM is 30 mA at 6.7 MHz in the active mode and 100 μA in the standby mode. The device operates at temperatures ranging from −40 to +85°C. The TC57512AD uses two high-speed programming modes with either 1-msec or 100-μsec program pulse widths. $12.35 (1000).

Toshiba America Inc, 9775 Toledo Way, Irvine, CA 92718. Phone local office.

Circle No 394

CLOCK-DRIVER IC

- *Available in 14-pin DIPs and SOIC packages*
- *Operates to 70 MHz*

The MC74F803 incorporates four flip-flops with inverting outputs sharing a common clock input. One of the four outputs is guaranteed a maximum rise and fall time of 1 nsec. Using this output as a divide-by-2 driver in a typical 68020/68030 application, a 66-MHz clock input

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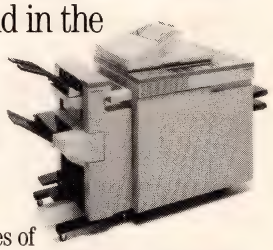

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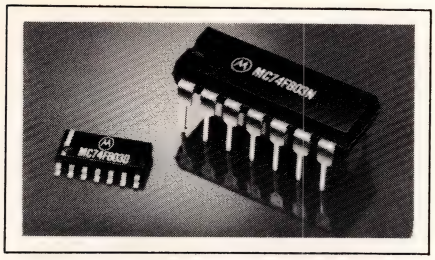

signal produces the 68020 clock with a maximum 1-nsec duty-cycle skew. The other three outputs have a duty cycle skew of 1.5 nsec max for less stringent requirements. When you use a 1-to-4 clock fan-out configuration, tight maximum skews of 1.5 and 3 nsec are also guaranteed for within-part and part-to-part devices, respectively. These configurations minimize clock skew in a multiple-clock system. Plastic 14-pin SOIC version, $8.45 (25).

Motorola Inc, Semiconductor Products Sector, Box 21007, Phoenix, AZ 85036. Phone (602) 962-2190.

INQUIRE DIRECT

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- *Drivers can sink as much as 64mA*
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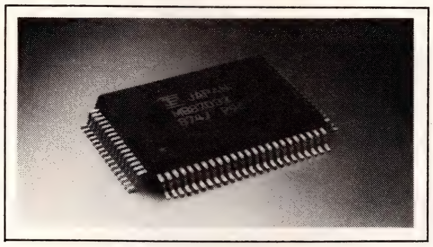
The MB87033B CMOS IC controls all the SCSI interface signals. The chip's onboard drivers/receivers provide direct connection to the SCSI bus, which eliminates the need for external drivers. And, by incorporating a 28-bit transfer byte counter, the controller optimizes performance and interface flexibility. The MB87033B is available in an 80-pin, gull-wing, plastic quad flatpack and in an 84-pin plastic leaded chip carrier. $14 (1000).



Fujitsu Microelectronics Inc, Integrated Circuits Division, 3545 N First St, San Jose, CA 95134. Phone (800) 642-7616; in CA, (408) 922-9000. FAX 408-432-9044.

Circle No 396

HIGH-RESOLUTION ADCs

- *Available as naked die*
- *Family has 12-, 14-, and 16-bit A/D converters*

Featuring an on-chip S/H circuit, the CS501x-U A/D converters are available in 0 to 70°C and −55 to 125°C temperature ranges. The CS5016-U provides 16-bit precision, No Missing Codes, an S/N ratio plus distortion of 92 dB, −100-dB peak harmonics, and offset errors of <1 LSB; this version also features a conversion time of >16.25 μsec and throughput rates as high as 50 kHz. The capacitor-based devices are self-calibrating to eliminate calibration drifts caused by handling and

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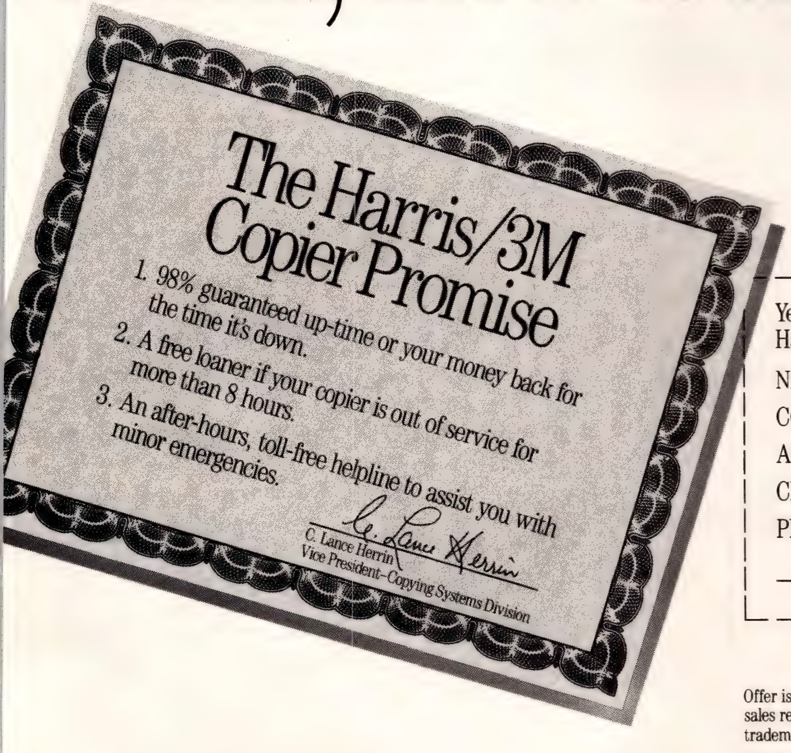

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CIRCLE NO 87

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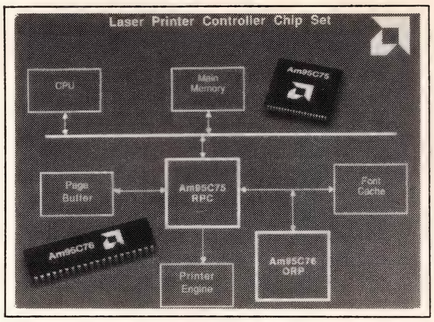
Crystal Semiconductor Corp, Box 17847, Austin, TX 78744. Phone (512) 445-7222. FAX 512-445-7581. TWX 910-874-1352.

Circle No 397

PRINTER CONTROLLERS

- *Can print as many as 45 pages/minute at 300 dpi*
- *Relieve CPU of bit-block transfer functions*



The Am95C75 raster-printer controller (RPC) and Am95C76 orthogonal rotation processor (ORP) laser-printer controller chip set are CMOS devices that free the controller board CPU of page-assembly tasks, font character rotations, and enable the CPU to handle complex page-description interpretations and graphics processing. The RPC employs a 3-bus architecture and a serial video port to reduce CPU bus traffic by performing simple bit-moving tasks without CPU intervention. The RPC builds and accesses a text cache, assembles the page with bit-precise alignment, provides dynamic RAM control of the page buffer, serializes buffer contents, and sends the data to the printer engine. In seven clock cycles, the RPC can do a bit-aligned read-modify-write. On the other hand, the ORP rotates characters and can print portrait or landscape documents as well as 2-sided documents. You can rotate the complete character set prior to printing or you can rotate the characters individually. RPC, $35; ORP, $12.65 (100).

Advanced Micro Devices Inc, Box 3453, Sunnyvale, CA 94088. Phone (408) 732-2400.

Circle No 398

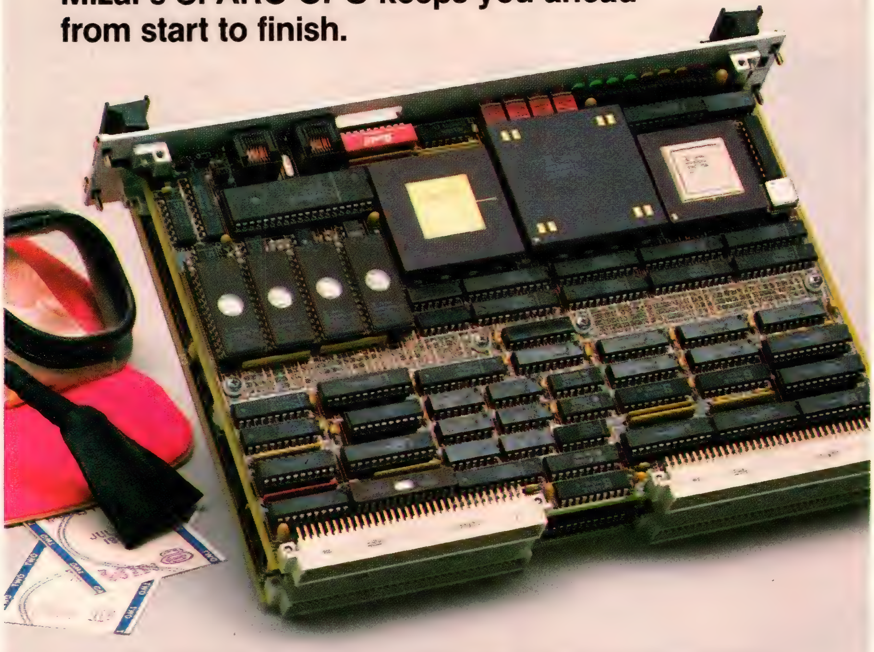
DUAL-GATE AMPLIFIER

- *DC requirements are 150 mA at 6V*
- *Accepts a positive supply voltage of 8V dc max*

The TGA8622-SCC monolithic, GaAs dual-gate FET has a typical performance of 7.5-dB gain and 20-dBm output power from 2 to 20 GHz. You can cascade the amplifier, which in a single stage provides a 30-dB gain control capability while maintaining a low input and output SWR. Gain versus frequency re-

Thoroughbred

Mizar's SPARC CPU keeps you ahead from start to finish.



You'll be favored to win with Mizar's MZ 7170, the VME processor with triple crown features. With the power of SPARC™ and the speed of zero wait-state SRAM, the MZ 7170 lets you run your application in record time. All for a price that keeps you on track.

The MZ 7170 was bred for demanding applications: a SPARC CPU at up to 25 MHz (15 MIPS), one MB of fast SRAM, up to four MB of EPROM, two RS-232 serial ports, mailbox interrupts, real-time clock, and optional T.I. 8847 FPU. And, the MZ 7170 is supported by a complete real-time operating system and UNIX®-based development tools.

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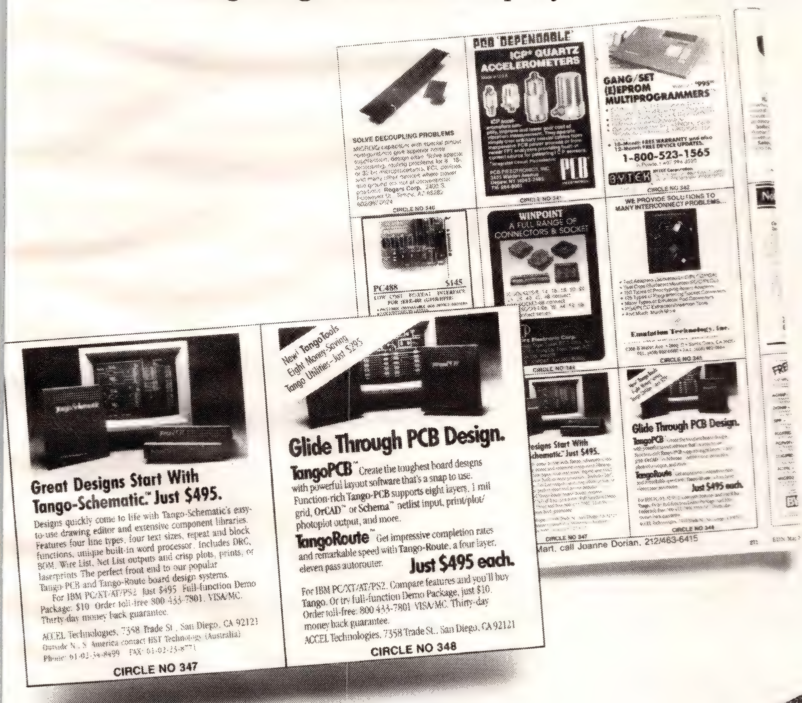
Raymond J. Schnorr
Vice President of Marketing
ACCEL Technologies

As Vice President of Marketing, Ray Schnorr is responsible for marketing ACCEL Technologies' affordable, professional software that meets the design needs of electrical engineers. He operates on a fixed budget and demands results. "When it comes to buying media, I'm interested in two things: performance and price. With EDN's Product Mart section, I pull high-volume sales leads and meet my budget," says Schnorr.

In nineteen months, ACCEL has sold 5000 software packages to 3000 sites. "Our ⅙-page Product Mart ads in EDN magazine are allowing us to reach our target audience." And Schnorr sees more for EDN and ACCEL. "We have significant growth plans for ACCEL, and running bigger ads in EDN will be part of the strategy to get there.

"The power and prestige of EDN is helping us grow into a leading design software company."



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CIRCLE NO 347

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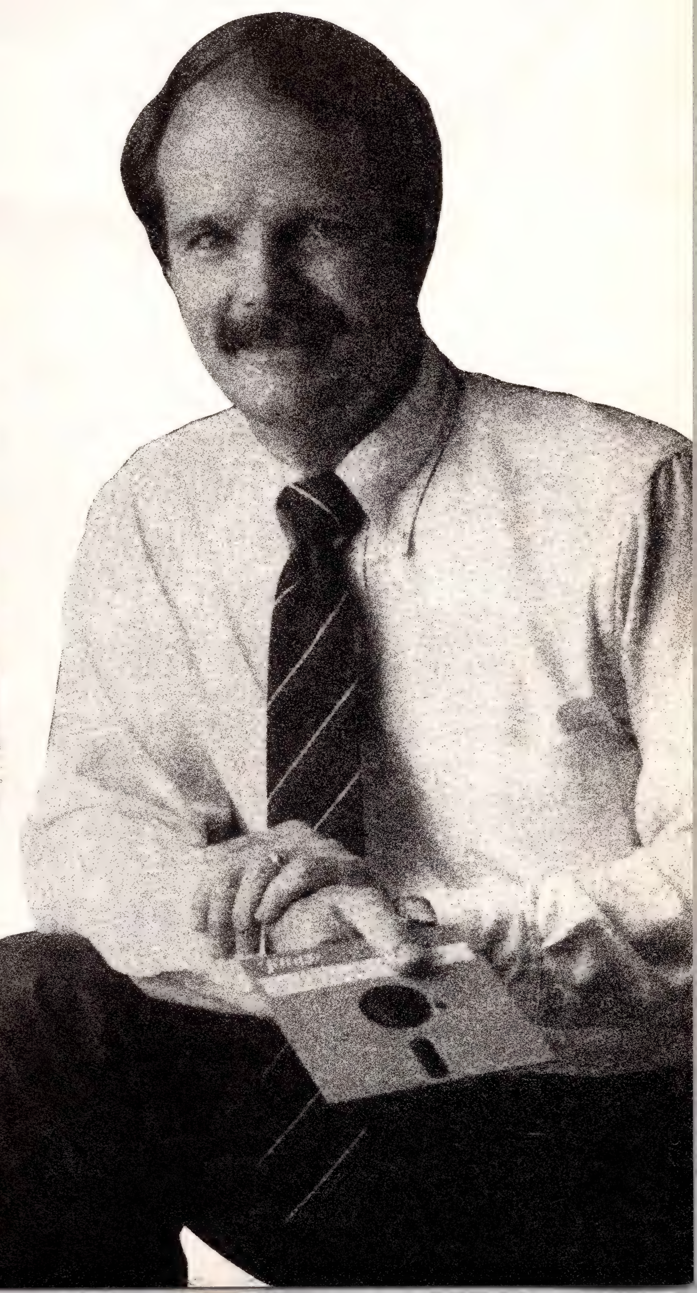

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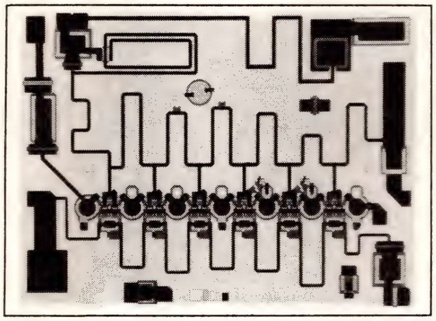
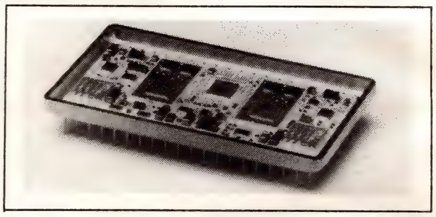
sponse varies no more than 1 dB for the first 15 dB of the gain-control range. The noise figure ranges from 6.5 dB at 2 GHz to 8.5 dB at 20 GHz. The output power at 1-dB gain compression is typically 20 dBm from 2 to 17 GHz and 16 dBm at 20 GHz. Input and output VSWR is less than 1.6:1 from 2 to 18 GHz and less than 2.3:1 from 2 to 20 GHz. The third-order intercept point ranges from 33.5 dBm at 2 GHz to 30.5 dBm at 20 GHz. The chip is 0.085 × 0.109 in. and has gold-plated bonding pads and backside, so you can use eutectic alloy-attach methods and thermocompression and thermosonic wire-bonding processes. Die, $64 (1001).



Texas Instruments Inc, Semiconductor Group (SC-872), Box 809066, Dallas, TX 75380. Phone (800) 232-3200, ext 500.

Circle No 399



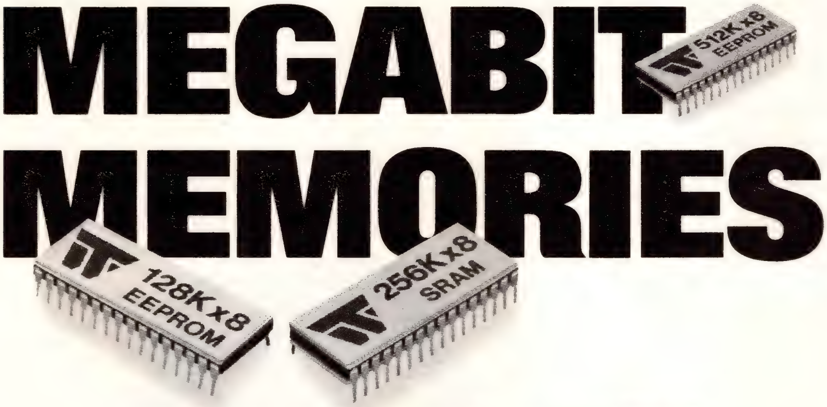
S/D CONVERTER

- *Has an accuracy of 0.0004 degrees*
- *Available in 40-pin DIP hybrid package*

The H2SD/H2RD1626 2-speed, 22-bit, tracking synchro (resolver)/digital converter operates off a 5V dc power supply and consumes 100 mW of power. The converter contains two independent type II servo loop tracking converters, along with a programmable 2-speed combiner. The speed ratio is pin-programmable by the user for eight standard binary and nonbinary ratios; specifically 8, 9, 16, 18, 32, 36, 64, and 72:1. Other features include built-in test, a reference synthesizer, an analog velocity output, and µP compatibility. The converter's anti-180° false lock-up circuit ensures that the converter does not get locked into an angle of 180° that's off the true angle when a 180° step function is applied. From $1145. Delivery, 12 to 16 weeks ARO.

Natel Engineering Co Inc, 4550 Runway St, Simi Valley, CA 93063. Phone (805) 581-3950. FAX 805-584-4357.

Circle No 400



MEGABIT MEMORIES

...in a 32-pin DIP!!

We've just packed a lot of CMOS memory into a single 32-pin DIP. You can now have 1 megabit (128Kx8) or 2 megabit (256Kx8) in SRAM or EEPROM with industrial or military temperatures. Our new high-density hybrid memories give you a choice. You'll also find that they'll lower your costs, save you board space, and conserve power, too.

Our rugged 1.6" x 0.6" ceramic package with JEDEC standard pinouts is brand new. Its welded metal cover and co-fired construction assures maximum integrity and hermetic seal, and lends itself to the most demanding industrial and military applications. MIL-STD-883 screening is available.

Want more? The EEPROMs offer a 10 Year Data Retention after write, and automatic page write option with internal address and data latches for up to 512 bytes, and 1 to 64 bytes/pages, up to 8 pages. Page write only 3.0mSec/page. And, there's data polling for end of write detection, and hardware and software data protection, too. Read access time is 150nSec.

The SRAMs include data retention with voltages down to 2.0 volts, read/write cycle compatibility with almost all microprocessors, and read access and write cycle times of 120nSec.

If 1 or 2 Megabit isn't enough, our 4 Megabit (512x8) will be out soon in the same 32-pin DIP. We also offer a range of access times down to speeds less than 50nSec, and memory capacities into the terabit region. Or, if you want to talk about products like a complex single-package system, a supercomputer array, or a totally defined multi-package management information system, give us a call. Your design or ours, we'll make it happen.

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CIRCLE NO 89

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For complete global coverage, Ehrsam places his advertising in EDN Magazine Edition and EDN News Edition. "Linear Technology Corporation is a strong supporter of EDN Magazine Edition. We rely on EDN's targeted coverage of the U.S. and Western Europe. When EDN News Edition added Pacific Rim circulation in December 1987, we added it to our media schedule."

For Bill Ehrsam, "EDN's Magazine and News Editions form the cornerstone for Linear Technology Corporation's media plan now and in the future."

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Model 199 System DMM
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- 500-point datalogging memory
- IEEE-488 interface standard
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Model 1992 Scanner Option
- Eight 2-pole channels or four 4-pole channels
- <1μV contact potential per contact pair
- 40 channel/second switching speed
- Factory or field installable
- **$395.**

CIRCLE NO 100

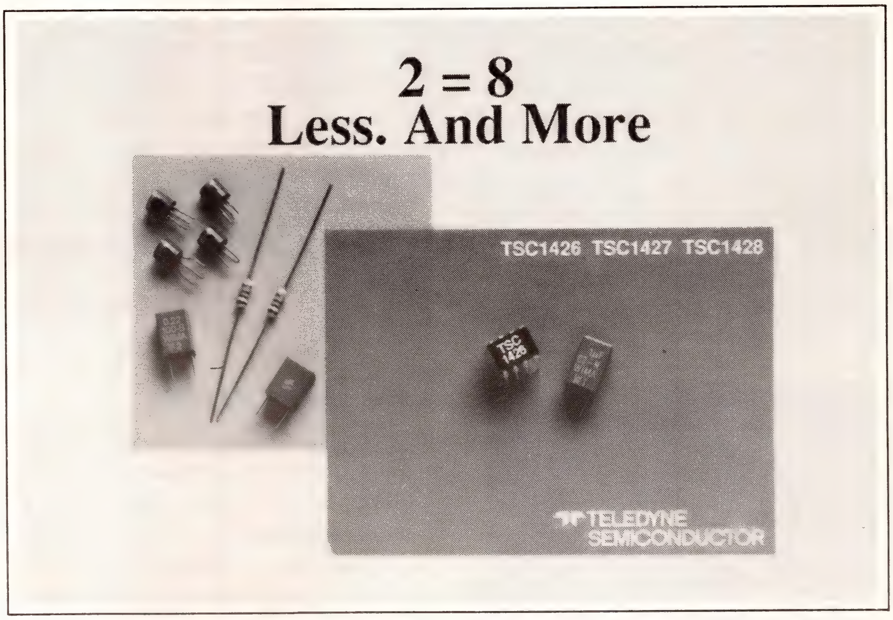
NEW PRODUCTS

COMPONENTS & POWER SUPPLIES

DRIVER MOSFETs

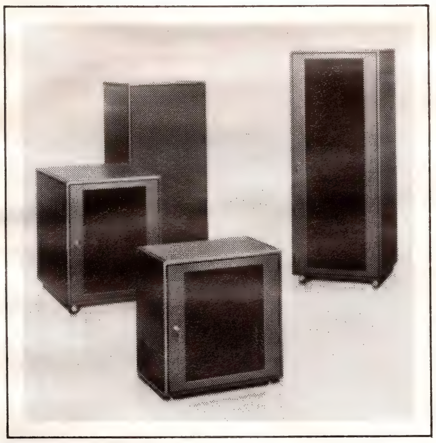
- *Can replace eight discrete MOSFET drive circuits*
- *Have 1.2A dual outputs*

Combined with one decoupling capacitor, just one of the drivers from the TSC1426-1428 family of MOSFET drivers can replace eight discrete components. The devices have dual 1.2A outputs and are available in inverting and noninverting configurations. The units are compatible with TTL, CMOS, or other input devices that develop a 2.4 to 18V level. The input requires no capacitors or resistive dividers to operate. The operating range spans 0 to 70°C. The drivers are fabricated on an epitaxial layer that makes them virtually latch-up proof. They're available in 8-pin DIPs and in surface-mount packages. TSC1426 unit, from $1 (100).



Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94039. Phone (415) 968-9241. TWX (910) 379-6494.

Circle No 401



ENCLOSURES

- *Shipped in kit form*
- *Feature simple assembly*

The lightweight 19-in.-wide cabinets in the Model 48 line feature a self-supporting frame made of aluminum die-cast parts. Easy to assemble, the cabinets offer mounting dimensions that conform to DIN 41494, part 1. The steel panels and doors are electrolytically galvanized with a textured brown-enamel finish. Side panels are available with or without ventilation slots. The units are shipped in kit form to reduce storage-space needs. Model 48 units come in heights of 21, 26.25, 31.5, 42, and 56 in. and in depths of 15.74, 23.62, and 31.5 in. Accessories include leveling feet, wheels, lifting eyes, grounding sets, dustproof seals, support rails, guide rails for sub racks, a fan tray, and a pull-out tray that can serve as a work bench. 21 × 15.74-in. unit, $350.

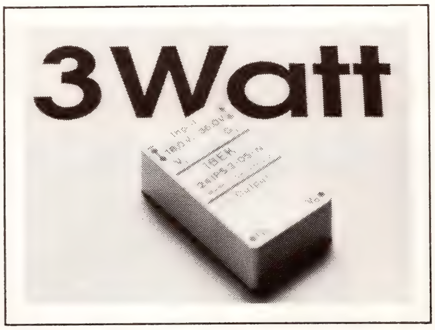
Elma Electronic Inc, 41440 Christy St, Fremont, CA 94538. Phone (415) 656-3400. FAX 415-656-3783.

Circle No 402

DC/DC CONVERTERS

- *Feature a 2:1 input range*
- *Provide a full-power output at 71°C*

The IPS family of 3W single- and dual-output dc/dc converters feature standard input ranges of 18 to 36V and 36 to 72V. Providing a full-power output over a −25 to +71°C range, the units are housed in a 24-pin DIP, which includes input and output filtering, and overvoltage and continuous short-circuit protection circuitry. Outputs of 5, 12, or 15V at current levels ranging to 500 mA are available. The typical conversion efficiency equals 80%, and the input-to-output isolation measures 500V dc. The output ripple equals 100 mV p-p, and the maximum no-load current measures 8 mA. $63 (100). Delivery, eight weeks ARO.



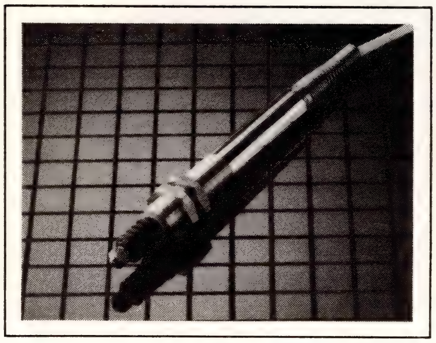
Melcher Inc, 200 Butterfield Dr, Ashland, MA 01721. Phone (508) 881-4715. FAX 508-879-8669.

Circle No 403

GAUGE HEADS

- *Have a ±0.1-in. adjustment range*
- *Are repairable*

LBB 100 gauge heads have a gauging-adjustment range of ±0.01 in. Pretravel and travel ranges are also adjustable so you can use a single head for various applications involving different measurement ranges. Positive mechanical stops prevent damage in case of overstroke. The heads feature a 2-piece construction and are repairable. The contact end of the device also has a removable tungsten carbide ball tip. The heads are available in threaded and unthreaded designs and operate from a 3.5V rms source. All units are configured with axial cable exits as standard, but 90° cables are available. Unthreaded versions, from $341; threaded versions, from $348. Available in March.

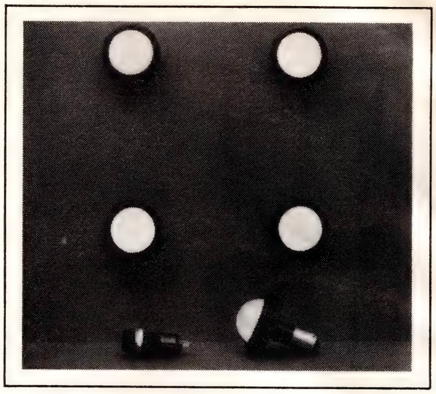


Schaevitz, Rte 130 & Union Ave, Pennsauken, NJ 08110. Phone (609) 662-8000.

Circle No 404

LED INDICATORS

- *Can replace incandescent lamps*
- *Available in six colors*

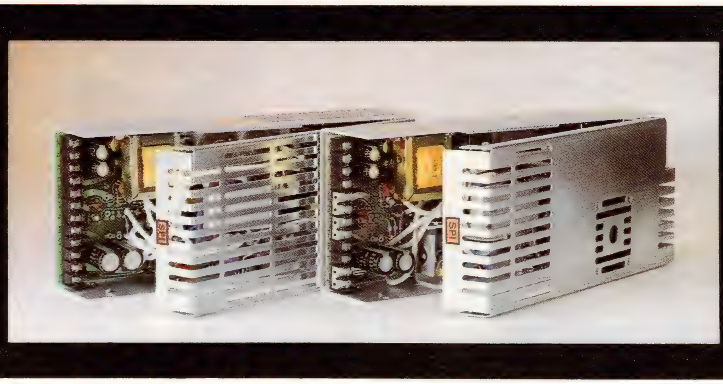


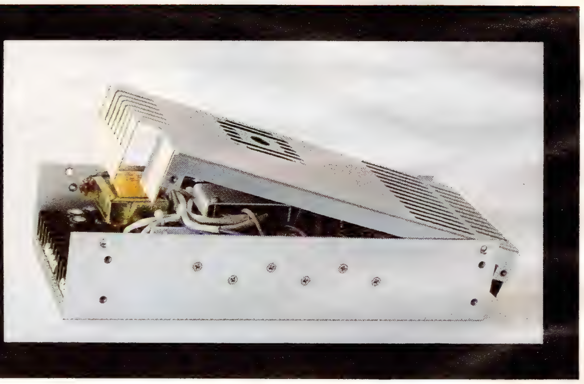
Bubble Light 20-mm LED indicators are designed to replace incandescent lamps. The units are easy to install in a variety of standard bases—miniature bayonet, flange, and screw. The LEDs are available in Hi-Efficiency red, red, orange, amber, yellow/green, and green. Milky-white-diffused or tinted-diffused lenses are available to match the LED color. Operating voltages range from 5 to 110V. With a 10-mA forward current, luminous intensities range to 40 mcd over the full 20-mm lens area. From $7 (1000). Delivery, 8 to 10 weeks ARO.

Data Display Products, Box 91072, Los Angeles, CA 90009. Phone (800) 421-6815; in CA, (213) 640-0442. FAX 213-640-7639.

Circle No 405

SO, IT'S POWER YOU WANT?





- 5 VDC at 70 Amps
- 12 VDC at 15 Amps
- 12 VDC at 5 Amps
- 24 VDC at 3 Amps
- 5 VDC at 3 Amps

- 5 VDC at 50 Amps
- 12 VDC at 6 Amps
- 12 VDC at 6 Amps
- 24 VDC at 3 Amps
- 5 VDC at 3 Amps

- 5 VDC at 30 Amps
- 12 VDC at 6 Amps
- 12 VDC at 3 Amps
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CIRCLE NO 92

DC/DC CONVERTERS

- *Have a wide input range*
- *Deliver 7.5W*

Offering single or dual outputs, HA Series converters offer a 7.5W output in a case measuring 2×2×0.375 in. Product features include a 4:1 input range, minimum efficiencies of 75%, a pi input filter to reduce reflected input ripple, and continuous short-circuit protection. The converters feature a 500V dc input/output isolation and a −25 to +71°C operating range. They're available in a package that features 6-sided continuous shielding. $43.20 (OEM qty).

Semiconductor Circuits Inc, 49 Range Rd, Windham, NH 03087. Phone (603) 893-2330. FAX 603-893-6280.

Circle No 406

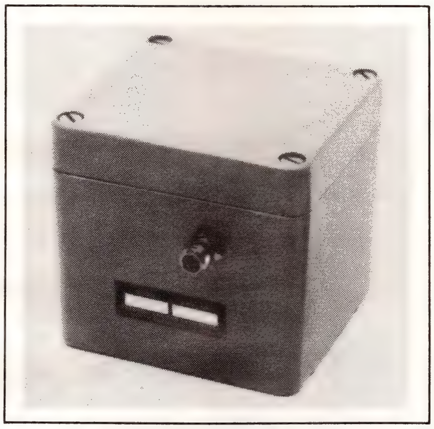
OPTICAL ENCODERS

- *Feature direct digital output*
- *Have a strain relief to protect the solder connections*

Type EO and EI panel-mount optical encoders feature a direct digital output that eliminates the need for A/D-conversion circuitry normally associated with analog inputs. Both units feature 256 quadrature outputs per revolution and have flatted shafts with through-holes for zeroing and centering. The encoders also employ a strain relief to protect the integrity of the solder connections. The EI encoders also have a third zero-reference output, which can be used to define a known reference point for starting an operation or process. EO encoder, $36.25; EI encoder, $47 (100). Delivery, stock to eight weeks ARO.

Allen-Bradley Co, 1414 Allen Bradley Dr, El Paso, TX 79936. Phone (915) 592-4888.

Circle No 407



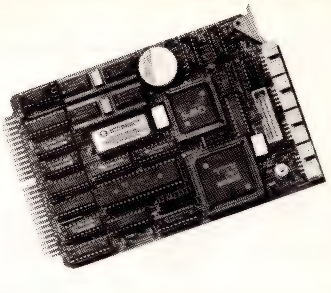
INCLINOMETERS

- *Boast ±1% accuracy*
- *Have a ±5 to ±90° measurement range*

HOC Series inclinometers are designed to measure the deviation from horizontal. According to the vendor, they have ±1% overall accuracy and are available with measurement ranges of ±5 to ±90°. Deviation from the horizontal produces an output that's directly proportional to the sine of the angle. The units are housed in a compressed polyester enclosure that can resist high shock and harsh environmental conditions. The devices weigh 300g. $315 (10).

Transducers & Systems, Box 185, North Branford, CT 06471. Phone (203) 481-5721. FAX 203-481-8937.

Circle No 408



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Use the 8500 as a **stand-alone** card or as a gateway to more than 1,000 industrial peripheral cards already available on the STD Bus. Write your application program in any PC language and run it on the STD Bus. Boots from on-card ROM disk. MS-DOS™ ROM option.

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- COM1 and COM2 serial ports
- LPTI printer port
- Battery-backed, calendar clock
- 128K static RAM
- 128K RAM/ROM disk
- 7.15 MHz V20 CPU
- Phoenix™ BIOS
- IBM PC compatible chipset
- Low power, 100% CMOS

EXPANDABILITY

Add up to 16 Mbytes of RAM/ROM disk for reliable operation in the industrial environment. Floppy, hard disk and video optional.

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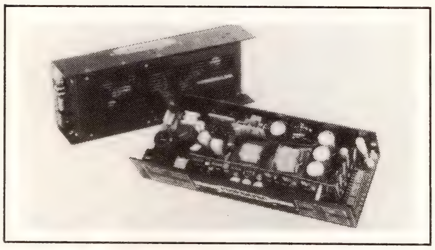
MEMBER STDMG STD MANUFACTURERS GROUP

CIRCLE NO 93



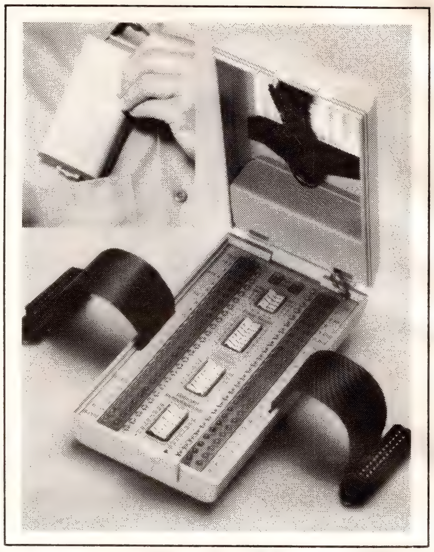
POWER SUPPLIES

- *Provide five isolated outputs*
- *Meet FCC and VDE EMI specs*

Units in the 29D5 Series switching power supplies provide five isolated outputs ranging from 5 to 48V and a 300W total power rating at 50°C. The main output is rated for 5V at 40A. Outputs 2, 3, and 4 provide 12 or 15V at 3 or 5A. The semiregulated output 5 can be either 12, 24, or 48V at 6, 4, or 2A, respectively. Line regulation for the field-selectable 90 to 132V ac or 180 to 264V ac inputs equals 0.2%. Load regulation for inputs 1 through 4 also equals 0.2%. Output ripple and noise is 1% p-p. When equipped with an optional filter, the supplies meet the requirements of FCC 20780 Class A and VDE 0871 Class A EMI specifications. $389.

Powertec, 20550 Nordhoff St, Chatsworth, CA 91311. Phone (818) 882-0004. TLX 277483.

Circle No 409



BREAKOUT BOX

- *Has 100-light capability*
- *Fits in a shirt pocket*

Designed with economy in mind, the Model 100H breakout box monitors the RS-232C interface. Compact enough to fit in a shirt pocket, it has a 100-light capability. The box provides instant line status (mark, space, data, clocking, or no-activity) with separate red and green LEDs. It is signal powered and has full interface definition with the 4-state LED indicators. In addition, the unit has loop-back and null-modem switches and a battery that can force control lines and check cables. A test probe lets you use the box as a 25-conductor cable checker. $219.

Datacom Technologies Inc, 11001 31st Place W, Everett, WA 98204. Phone (206) 355-0590. FAX 206-353-9292.

Circle No 410

5 Good reasons you should use YSI thermistors to measure temperature.

1. **High sensitivity.** YSI thermistors have a wider response to temperature changes than other types of sensors. One of our typical thermistors changes 1,290 ohms/°C at 25°C, which produces highly accurate measurements.

2. **Tight tolerances.** YSI thermistors offer standard interchangeabilities of ±0.2°C and ±0.05°C.

3. **Ruggedness.** YSI thermistors are working deep under the ocean and on a mission to Mars.

4. **Hermetic seal.** In severe moisture environments, YSI glass-encapsulated thermistors typically drift an insignificant 0.60°C at 200°C in 100 months.

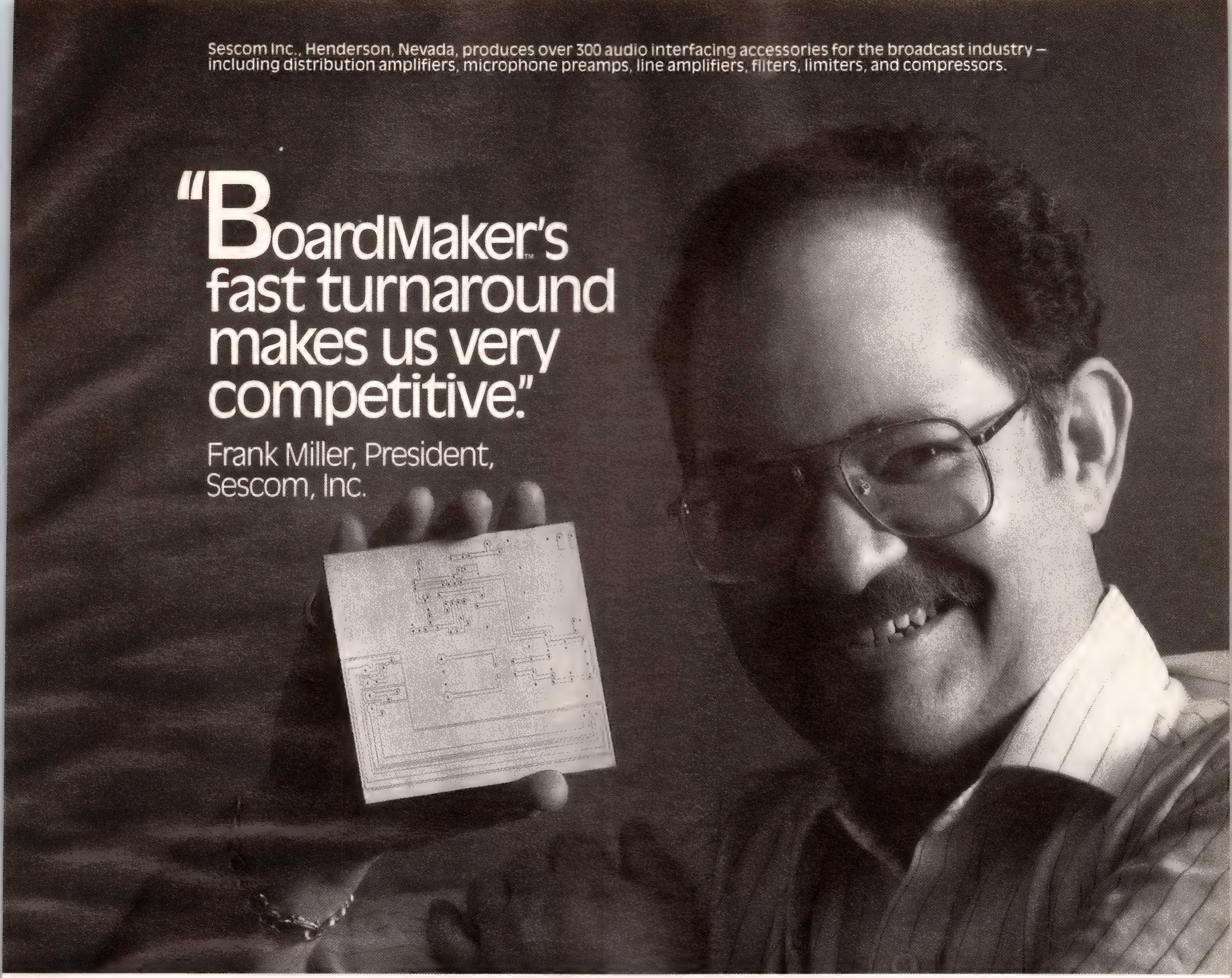
5. **Flexible packaging.** Order YSI thermistors unmounted, select complete assemblies from 41 standard packages, or have us build you custom probes.

Find out all the good reasons for specifying YSI by asking for our catalog and Application Notes. Call **toll-free 800 343-HELP** (or 513 767-7241).

YSI Incorporated
Yellow Springs, Ohio 45387 USA

CIRCLE NO 94

Sescom Inc., Henderson, Nevada, produces over 300 audio interfacing accessories for the broadcast industry – including distribution amplifiers, microphone preamps, line amplifiers, filters, limiters, and compressors.



"BoardMaker's™ fast turnaround makes us very competitive."

Frank Miller, President,
Sescom, Inc.

"Half our business is rush. This week, every week. We never know what we're going to design or modify. So fast reaction time is critical for us.

"That's where the BoardMaker comes in. It lets us react with finished circuit board designs in hours instead of days. And that makes us very competitive.

"The ability to make more changes in a given time frame.

If you send out for etched boards, there is a tendency to make do with what you thought you needed. But with the BoardMaker, you are spurred to make boards perfect—make little fixes here and there—because you can do it without waiting.

"A short cycle from brain to hardware.

With this machine, you get the finished prototype in front of you while the design is still fresh in your brain. Then you can polish the design—before your idea has turned to tapioca.

"Runs seven hours a day, five days a week.

The BoardMaker is also a good small lot production tool. We run it all week long, making boards from a half-inch square up to six inches by eleven. Most are single-sided.

"Changes during production runs? No problem.

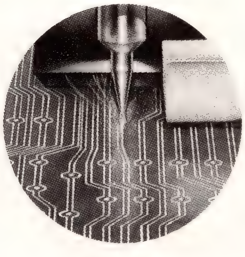
Sometimes we have to substitute components. Or make short run specials for customers. With the BoardMaker, we just make the change and keep going.

"An affordable system.

The cost is very affordable. And we're very happy avoiding the astronomical costs involved when we sent things out on a rush basis (and still forgot about half of what we were going to do)."

See us at NEPCON WEST, Booth #2348

CIRCLE NO 71



Three BoardMaker models make single- and double-sided boards for prototyping or small production runs. Cost is much less than first-generation machines; milling speed is faster. For information, call 415 883-1717 or mail the reader card. Or send $12.95 for an all-features demo on VHS cassette.

Instant Board Circuits
20A Pamaron Way
Novato, CA 94949

ibc
Instant Board Circuits

When size and speed matter, Look to Seagate's 3.5″ ST157 Family

When 5.25″ drives won't fit, or if you just think "small is beautiful," Seagate's ST157 family provides less than 30 msec access time for today's generation of high-performance personal computers.

Select from the 21 MB ST125, the 32 MB ST138 or the 48 MB ST157, all available with either SCSI or ST412 interface options.

With over one million produced, Seagate now builds over 8,000 ST157 family drives per day. And each one is built with the quality and reliability you've come to expect from the first name in disc drives.

For easier installation, you can configure the right 3.5″ solution by choosing from Seagate's line of controllers and adapters for the ST157 family.

For more information on the small drives that are big on speed, contact your authorized Seagate Distributor, or call Seagate at 800-468-DISC.

CIRCLE NO 97

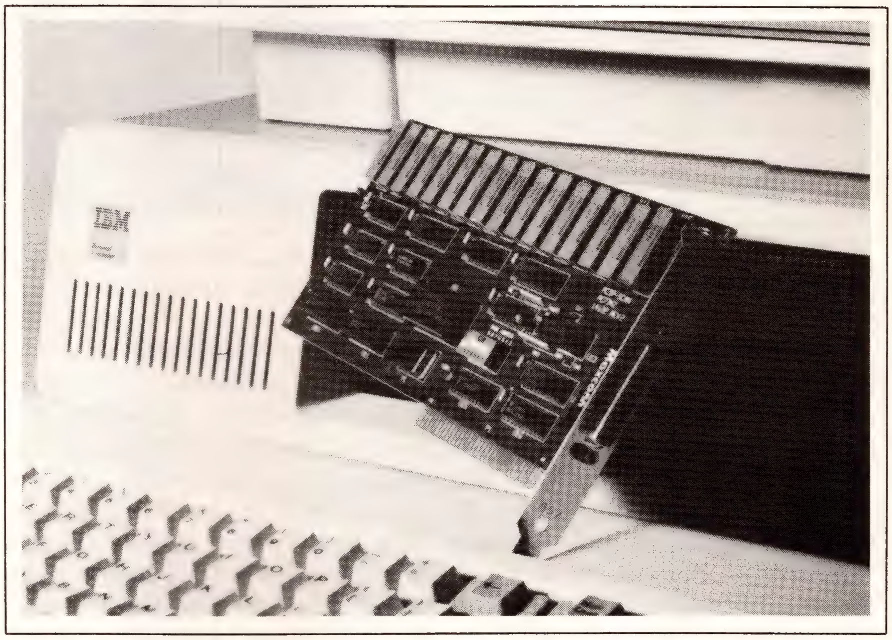
Seagate
The first name in disc drives

NEW PRODUCTS

COMPUTERS & PERIPHERALS

RELAY SCANNER

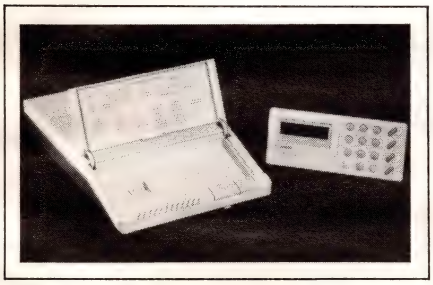
- *Multiplexer board for the IBM PC, PC/XT, and PC/AT*
- *Features 16 mercury amalgam nonposition sensitive relays*



The PCIP-Scan reed-relay scanner and multiplexer for the IBM PC, PC/XT, PC/AT, and compatible computers features 16 mercury amalgam nonposition sensitive relays for each of its 16 inputs. The card can be configured as 16 single-ended or eight differential input channels. During a scan each input relay is de-energized for 3 msec to guarantee break-before-make switching. This time delay is followed by a 3-msec debounce settling time. Following the settling period, a trigger signal is sent to an external pin that can trigger an external ADC. You program the board, using language-independent commands. The software consists of device drivers that load into the computer each time it reboots. A pop-up display of the card's status, which the user activates by a hot-key sequence, occupies only one-third of the screen. $325.

Metrabyte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. FAX 508-880-0179. TLX 503989.

Circle No 351



CCITT V.32 MODEM

- *Conforms to V.22bis, V.22, and Bell 212AR, 103/113 specs*
- *Upgradable personality module guards against obsolescence*

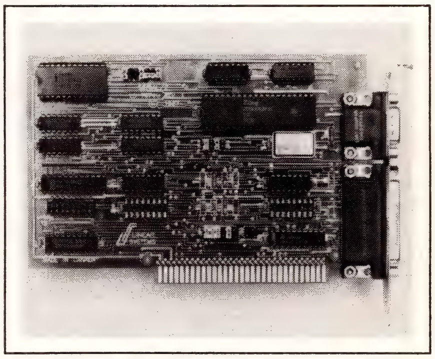
The N9635 modem conforms to the CCITT V.32, V.22bis, V.22, and the Bell 212AR, 103/113 specifications. An optional display/control module (D/CM) contains 32k bytes of battery-backed static RAM that provide storage for two modem configurations; an 8031 microcontroller lets the user run advanced diagnostics, such as signal-quality monitoring, S/N ratio, and bit-error tests, at local or remote locations. In addition, the upgradable personality module can incorporate changes as modem standards and capabilities evolve. The module contains as much as 512k bytes of ROM and a Z80 μP. The modem can communicate at 19.2k bps when utilizing its Microcom Networking Protocol Class 5 algorithm for data compression. $1495. Optional D/CM, $150.

NEC America Inc, Data and Video Communications Systems Div, 110 Rio Robles, San Jose, CA 95134. Phone (800) 222-4632, ext 1277; in CA, (408) 433-1250.

Circle No 352

SERIAL INTERFACE

- *Board for the IBM PC/AT provides dual channels*
- *Uses the 82530 serial communications controller*



The LSPC Serial/2 dual-channel multiprotocol serial interface board for IBM PC/AT computers utilizes the Intel 82530 serial communications controller (SCC) so that each channel can support communications with a data terminal, a modem, an X.25 network, or a T1 gateway. You can also insert interface chips in resident sockets to meet the electrical standards for RS-232C/RS-422 and RS-485 communications. You can program the SCC to handle synchronous and asynchronous modes. An external signal or an internal phase-locked loop can be used as the clock in the synchronous mode. Optional interrupt and

DMA configurations are available to handle high-speed communications on channel A. A 3-byte receive buffer on each channel handles extended CPU response times. $245.

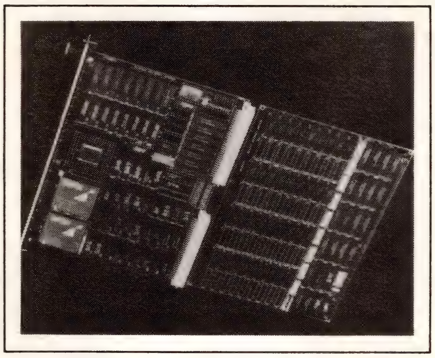
Computer Modules Inc, 2348C Walsh Ave, Santa Clara, CA 95051. Phone (408) 496-1881. FAX 408-496-1886.

Circle No 353

ACCELERATOR MODULE

- *For IBM PC/AT bus, Q Bus, and VME Bus computers*
- *64-bit floating-point unit and 32-bit integer processor unit*

The MC6400 accelerator module for IBM PC/AT bus, Q Bus, and VME Bus computers consists of two boards that plug together so that they occupy a single slot in the host. The module utilizes the Weitek XL-8064 chip set, which provides a 64-bit double-precision floating-point unit and a 32-bit integer-processor unit. The unit achieves a 10-MIPS and 20M-flops (double-precision) performance rating. It accelerates C and Fortran applications containing a high percentage of floating-point computations. In addition, the module contains a program sequencer unit, 4M or 8M bytes of 2-way interleaved memory, an 8k × 64-bit instruction cache and host-interface logic. The unit has a 64-bit data bus connecting the processing units with the main memory, which transfers data at 80M bytes/sec. A variety of optional software is available including Vast-2, which optimally compiles a Fortran program by detecting vector and concurrent operations. 4M-byte version, $16,450; 8M-byte version, $20,450.



Mercury Computer Systems Inc, Wannalancit Technology Center, 600 Suffolk St, Lowell, MA 01854. Phone (508) 458-3100. FAX 508-458-9580.

Circle No 354

ROM DISK DRIVE

- *Offers a 400-msec access time*
- *Holds 680M bytes of data*

The XM-3201A compact-disk ROM drive has an average access time of 400 msec. It comes with hardware and software to operate with IBM PC/ATs, PC/XTs, and compatibles; PS/2s; and Macintosh computers. The drive includes a controller, a SCSI interface, a power supply, and external drive packag-

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ing. The disk drive accepts the industry-standard cartridge, which holds 690M bytes of information. The unit also has an integral audio capability that allows you to combine high-fidelity stereo sound with text and images. $1095.

Toshiba America Inc, Disk Products Div, 9740 Irvine Blvd, Irvine, CA 92718. Phone (714) 583-3108.

Circle No 355

COPROCESSOR BOARD

- *Uses a 10-MHz 80186 μP for IBM PC/XT and PC/AT*
- *Combination board provides one parallel and four RS-232C ports*

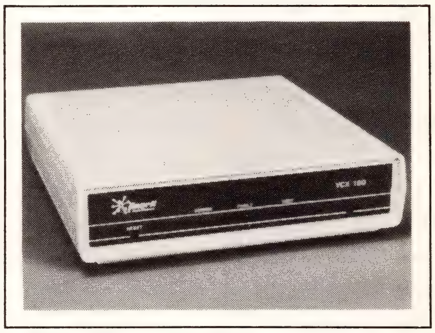
The DCP-186/PC coprocessor board for the IBM PC/XT, PC/AT, and compatible computers consists of a plug-in board and a daughter card. The plug-in board contains a 10-MHz 80186 μP, which provides timers, an interrupt controller, and DMA controllers. The board also contains 128k or 512k bytes of memory. The daughter card supports four RS-232C ports, a Centronics parallel-printer port, and a port termination box containing serial and parallel connectors. The unit has a shared-memory interface, 2-way interrupts, and support for synchronous communications on all lines. From $1395.

Emulex Corp, Box 6725, Costa Mesa, CA 92626. Phone (800) 368-5393; in CA, (714) 662-5600.

Circle No 356

MULTIPLEXER

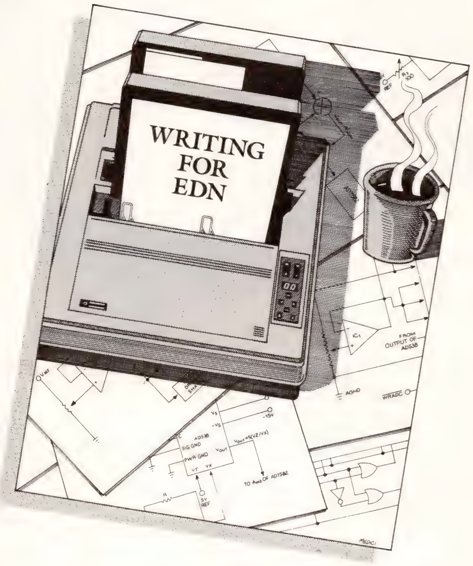
- *Features either 8 or 16 ports*
- *Can function as a small PBX*



The VCX-100 8- or 16-port switching statistical multiplexer can serve as either a small data PBX or a simple point-to-point statistical multiplexer when connected to another VCX-100. The multiplexer features port selection and contention, dual sessions with hot-key toggle, an inactivity timer, transparent operation, a system logger, channel priority, speed conversion, flow-control conversion, local echo, automatic connections, access control, statistical reporting, port and trunk diagnostics, parity conversion, and full break handling. You can configure the unit for software control. 8-port model, $1495; 16-port model, $2195.

Penril DataComm, 207 Perry Parkway, Gaithersburg, MD 20877. Phone (301) 921-8600.

Circle No 357



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LIGHT PEN/BOARD

- *Provide 1024 × 768 pixels for IBM Micro Channel*
- *Software driver lets you use light pen in Windows applications*

The FT-1000 light pen connects to the PXL-480, which is a plug-in board for IBM Micro Channel computers. The FT-1000 uses surface-mount technology to obtain a 42% smaller profile than its predecessor, the FT-156. A reconfigured cord reduces the weight and pull at the back of the pen. The PXL-480 board fits into a video slot in the PS/2 computer. The board and its accompanying software provide a resolution as high as 1024 × 768 pixels. An optional cable lets you install the board in any available slot, and a software driver for Microsoft's Windows lets you run Windows applications, using the light pen. In addition, the software includes a driver for AutoCAD and an emulation of Microsoft's mouse interface. FT-1000, $249; PXL-480, $179.

FTG Data Systems, 10801 Dale St, Suite J-2, Stanton, CA 90680. Phone (800) 962-3900; in CA, (714) 995-3900. FAX 714-995-3989.

Circle No 358

VME COMPUTER

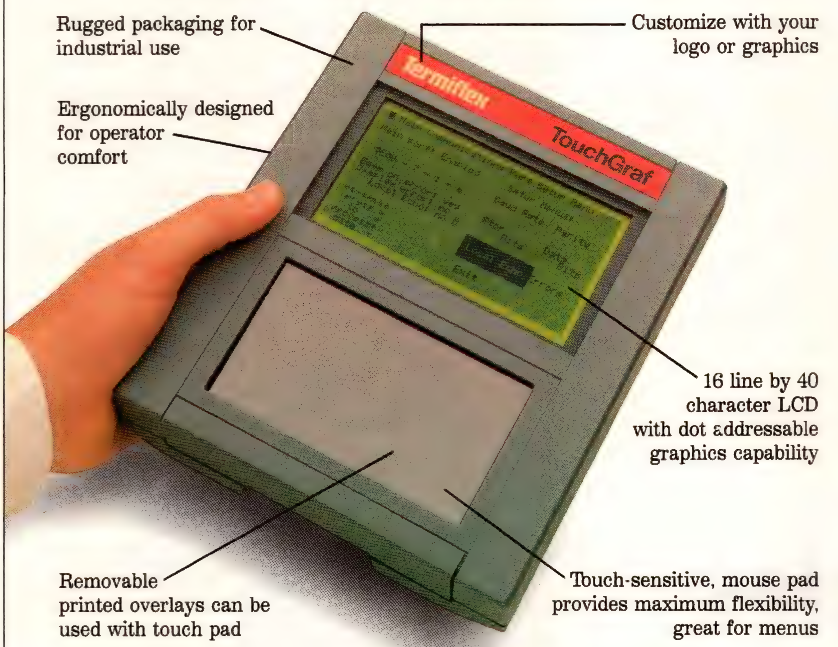
- *Runs at 20 or 25 MHz*
- *Offers extensive I/O options*

Based on the 68030, the VPU-30 CPU board runs at 20 MHz with zero wait states or at 25 MHz with one wait state. Providing as much as 8M bytes of onboard, dual-ported memory and an optional 68882 floating-point coprocessor, the board can serve as a stand-alone µC, a single CPU/controller in a VME Bus system, or one of many CPU elements in a multiprocessor system. The VPU-30 includes dual universal-protocol serial communication ports, modem support, onboard FIFO SCSI support that offloads the CPU's interrupt load, and RS-232C and RS-422 serial line levels. The board also provides IEEE P1014 VME Bus compliance. It features a fully programmable VME interface and offers A:32, D:32 specifications for bus and memory access. $3555 (100).

SBE Inc, 2400 Bisco Lane, Concord, CA 94520. Phone (800) 221-6458; in CA, (800) 328-9900. FAX 415-680-1427.

Circle No 359

Keyless Keypad Makes TouchGraf™ The Next Generation of Flexible Terminals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Touch-sensitive, mouse pad provides maximum flexibility, great for menus

TouchGraf's large display and touch pad give you great flexibility. Menu choices are displayed on the large screen by the terminal or host software, and the operator touches the corresponding touch pad area to select his choice. An on-board battery and up to 192K of RAM are available for data storage.

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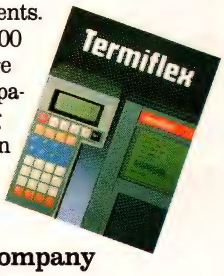

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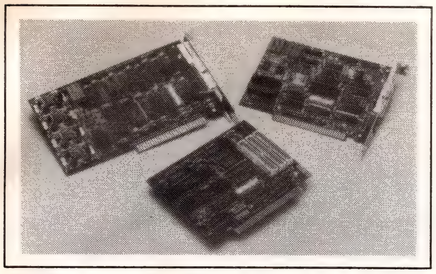
CIRCLE NO 99



ACQUISITION BOARDS

- *Plug into IBM PCs and compatibles*
- *Handle digital and analog data*

The vendor's three single-board data-acquisition systems plug into IBM PCs and compatibles, 386-type machines, and IBM PS/2s (Model 30). The PCI-20087W-1 digital I/O board offers 40 channels of TTL-compatible signals. With software, you can independently program each 8-bit channel grouping for use as either an input or an output port. The PCI-20087W-1's operating speeds range to 360k bytes/sec. The PCI-20089W-1 analog-input board accommodates either 16 single-ended or eight differential channels. The system includes an internal timebase generator and an auxiliary pulse counter, and it features 12-bit resolution, software-controlled gains, and a 32-kHz sample rate. The PCI-20093W-1 is an analog output board that includes eight voltage or current channels with a total throughput of 31,200 outputs/sec max. It employs a refreshing technique that provides error-free updates to all eight channels within 256 µsec. PCI-20078W-1, $165; PCI-20089W-1, $495; PCI-20093W-1, $495.

Burr-Brown Corp, 1141 W Grant Rd, MS-131, Tucson, AZ 85705. Phone (602) 746-1111.

Circle No 360

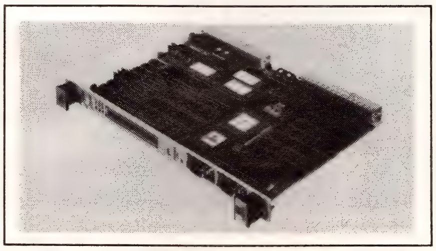
INDUSTRIAL PC

- *Contains an 8-MHz 80286 µP and 1M byte of RAM*
- *Unit operates over a 32 to 131°F range*

The DataTough 286 industrial computer is based on an 8-MHz 80286 µP. A base unit contains 1M byte of RAM, a 720k-byte, 3½-in. floppy-disk drive, a 20M-byte hard disk, two serial ports, one parallel port, three available 16-bit slots, a travel-sealed keyboard, and a monochrome monitor capable of 720×348-pixel resolution. The unit can operate over a 32 to 131°F range in humidity levels of 5 to 95%. In addition, the unit can withstand shocks as high as 10g during operation. The unit is built with heavy-gauge aluminum, and all openings are sealed with gaskets. The keyboard is made of a contaminant-resistant membrane. The computer measures 11×21×18-in. and weighs 65 lbs. $4950.

Cimpoint, 1807 W Braker Lane, Suite S, Austin, TX 78758. Phone (800) 622-2993; in TX, (512) 837-3707.

Circle No 361



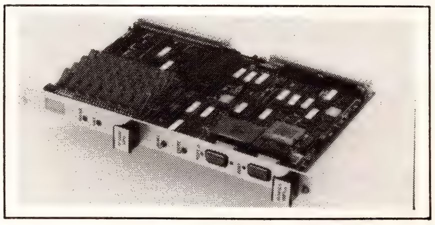
VME CPU BOARD

- *Uses a 33-MHz 68030 µP operating with no wait states*
- *Provides as much as 2M bytes of quad-ported static RAM*

The 68-33 VME Bus board is based on the 68030 µP operating at speeds as high as 33 MHz with no wait states. The board contains as much as 2M bytes of quad-ported static RAM, which is tailored for multiprocessing. A local µP bus connects to the 68030, a coprocessor, and the static RAM. An I/O and memory bus links the I/O functions to the VME Bus and a VSB interface. This bus also connects to the static RAM, permitting DMA transfers from the VME, VSB, or I/O devices without µP intervention. The board uses VTC's VIC068 VME Bus interface controller chip and a custom VSB interface circuit, which permits high-speed DMA transfers. You can optionally install as much as 512k bytes of EPROM for application code and 2k bytes of battery-backed static RAM. The board also has a 32-bit auxiliary bus, Apex, which lets you add additional functions such as SCSI, IEEE-488, and parallel I/O ports. From $4595.

Radstone Technology, 1 Blue Hill Plaza, Pearl River, NY 10965. Phone (800) 368-2738; in NY, (914) 735-4661.

Circle No 362



VME CPU BOARD

- *Has 16-MHz 68020 µP and 4M bytes of dynamic RAM*
- *Transfers data at 30M bytes/sec to onboard dynamic RAM*

The IV-3220 CPU board for the VME Bus contains a 16-MHz 68020 µP and 4M bytes of dual-ported dynamic RAM. A static-column block-transfer mode permits 30M-byte/sec data transfers into the onboard memory. In addition, the board contains a 16-bit programmable counter, two serial I/O ports, mailbox interrupts, a software reset, a VME1000 VME Bus system controller, and an option for a 68881 floating-point coprocessor. An optional daughter card provides a VSB interface. You can install the board in the company's Performer 32A Unix system as a real-time node in multiprocessing applications. A variety of software tools are available for developing real-time multiprocessing systems. $2995 (100).

Ironics Inc, 798 Cascadilla St, Ithaca, NY 14850. Phone (607) 277-4060. TLX 705742.

Circle No 363

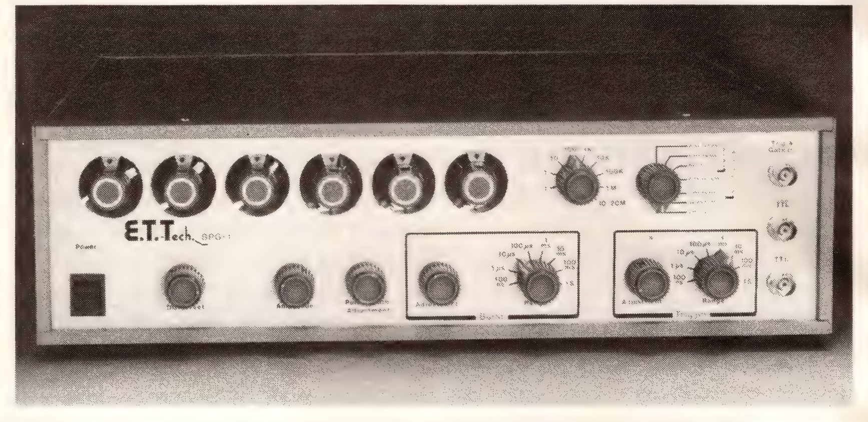
NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

PULSE GENERATOR

- *Provides two output signals*
- *Digitally accurate pulse trains have pulse-width control*

The PSG-20 pulse-generator/synthesizer combines digital and continuous analog control and can synthesize frequencies from 0.1 Hz with 0.1-μHz accuracy to as high as 20 MHz with accuracy to a few cycles per second. Separate delay and burst signals are continuously adjustable in each of eight decade ranges from 10 sec to 100 nsec. The pulse-generator/synthesizer provides two output signals—a TTL output and an adjustable 20V p-p, 50Ω, 1500V/μsec slew-rate output with dc offset. $1245.



E T Tech Inc, 15 S Van Brunt St, Englewood, NJ 07631. Phone (201) 569-3339. TLX 642145.

Circle No 375

PORTABLE RECORDER

- *Weighs 11 lbs*
- *Battery provides 10 hours of continuous operation*

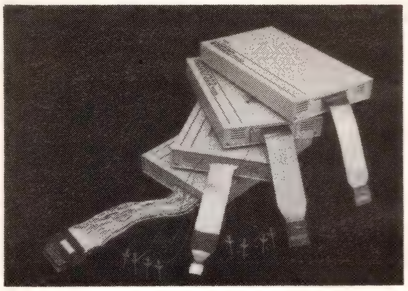
The Series 4500 Microscribe analog strip-chart recorder provides 34 chart speeds and 18 sensitivity ranges, starting at 1 mV full scale. The recorder has 15 spans, a 100 cm/sec slew rate, and repeatability of better than 99%. A Houston Instrument capacitive rebalance transducer gives the recorder a 0.25-sec response rate. The device is microprocessor controlled and features continuous self-test. An optional battery pack provides a 24V supply. $1095.

The Recorder Co, Box 8, San Marcos, TX 78667. Phone (512) 353-5333.

Circle No 376

IN-CIRCUIT EMULATOR

- *Emulates CPU memories to 8.5M bytes*
- *Supports 68020, V60, and V25 μPs*



The SA98 in-circuit emulator supports real-time emulation of NEC's V60 32-bit CMOS μP and V25 16-bit CMOS μP at the processors' maximum clock speeds. The SA98 also permits single-step emulation and supports the 68020. Emulation memory, consisting of CMOS static RAM, is mappable in 4k-byte units, and is expandable to 8.5M bytes. You can add or modify breakpoints or trace trigger points or download new data into emulation memory without a CPU break or reset. A parallel bus enables high-speed data transfer from the host to the emulator or the target system. With 256k bytes of emulation RAM, $15,000 for V25 and 68020; $16,000 for V60. Additional RAM, $2700 for 256k bytes.

Sophia Computer Systems Inc, 3337 Kifer Rd, Santa Clara, CA 95051. Phone (408) 733-1571. TLX 853394.

Circle No 377

SMD-REPAIR KIT

- *Contains hot-air desoldering tool*
- *Uses nozzles that match most component outlines*

The surface-mount technology kit includes tools, supplies, and instructions for component replacement on surface-mount assemblies. It is housed in a transit case. Included in the kit is a hand-held, temperature-regulated, hot-air soldering/desoldering tool with three nozzles. Additional nozzles, matching the outlines of most surface-mounting components, are available. Also included are a videotape, a workbook, and a circuit board for developing the necessary repair skills. $1995.

John Fluke Mfg Co Inc, Box C-9090, Everett, WA 98206. Phone (800) 526-8731; in AK, HI, WA, (206) 356-5774.

Circle No 378

SCSI TESTERS

- *Issue commands; monitor and report target status*
- *Support 167 bus functions*

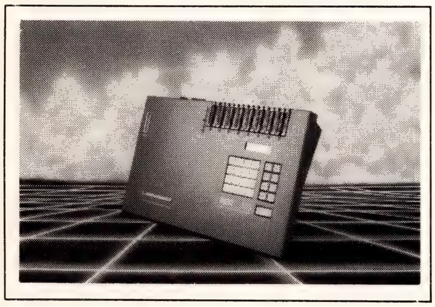
The IPC-5000 and IAM-5000 are SCSI testers. The first unit is packaged as a full-length card that plugs into the IBM PC bus; the second

Text continued on pg 211

is a complete tester based on the Ampro Little Board 186 MS-DOS-based computer. Both testers support bus transfers at 5M bits/sec. The testers act as SCSI initiators and can also emulate target devices on the bus. In normal operation, they issue commands and phasing sequences and monitor and report the responses of the unit(s) under test. Currently, the expanding library of supported bus functions includes 167 items. The Little-Board-based tester performs all functions of the PC-based unit except for synchronous transfers, hardware data comparison, parity-error insertion, and variable delay. IPC-5000, from $3800; IAM-5000, from $2500.

I-Tech, 12545 Tussock Ct, Eden Prairie, MN 55344. Phone (612) 941-5905.

Circle No 379



PROGRAMMER

- *Expands to program 40-pin PLDs and μPs*
- *Programs EPROM sets; gang-duplicates EPROMs*

The model 135-H Multiprogrammer is a gang/set EPROM programmer for groups of eight 32-pin devices. As an option, you can equip the unit to program 40-pin PLDs and μPs, 3-voltage EPROMs, and bipolar PROMs. You can also use the instrument as an 8- or 16-bit EPROM emulator. You can operate the programmer in stand-alone mode—it includes a 40-character LCD and a 25-key full-travel keypad—or you can use it with an external terminal or computer; both a parallel printer port and an RS-232C port capable of data rates from 150 to 38.4k bps are standard. The unit includes 512k bits of RAM that you can expand to 4M bytes. Software that runs on IBM PCs and compatible computers allows editing of PROM contents and use of the PC for data-file storage. From $1395.

Bytek Corp, 508 NW 77th St, Boca Raton, FL 33487. Phone (407) 994-3520. FAX 407-994-3615.

Circle No 380

FUNCTION GENERATORS

- *Range of output waveforms at frequencies to 20 MHz*
- *Available with sweep-frequency capabilities*

The TG2001 and TG2002 are 20-MHz function and sweep-frequency function generators, respectively, that generate sine, triangle, ramp, pulse, haverwave, or dc output

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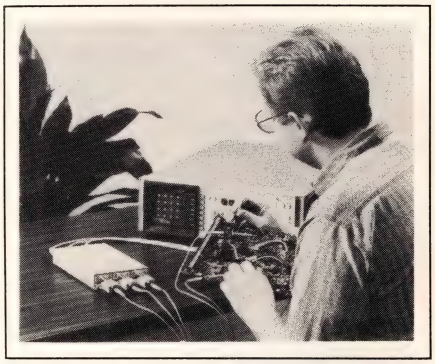
CIRCLE NO 102

waveforms from a 50Ω output. A single-turn vernier control and a 3-position switched attenuator allow you to control the output amplitude over a 60-dB range with a maximum output amplitude of 20V p-p. You can also introduce a dc offset in the range of ±10V into the output. The generators have a TTL-level output. Separate coarse- and fine-control verniers and an 8-decade range multiplier allow you to select output frequencies between 0.002 Hz and 20 MHz. Both the verniers and the instrument's sweep-frequency input provide 1000:1 frequency control. The generators have free-run, triggered, or gated operating modes, a variable start/stop phase, and 19:1 output symmetry control. The TG2002 includes linear or logarithmic frequency-sweep facilities, with the sweep limits set by the vernier controls and stored digitally to eliminate drift. TG2001, £595; TG2002, £845.

Thandar Electronics Ltd, 2 Glebe Rd, Huntingdon, Cambridgeshire PE18 7DX, UK. Phone (0480) 412451. TLX 32250. FAX 0480-411463.

Circle No 381



PROBE SYSTEM

- *Covers dc to 250 MHz with 1-mΩ and 8-pF loading*
- *Works with HP 8980A and 8981A vector-modulation analyzers*

The HP 11748A is an active probe system with three probes for use on densely packed modules of radar and communications systems. You can trace in-phase and quadrature analog signals through amplifiers and filters while simultaneously using the third probe for triggering. The maximum input signal voltage is ±1V or ±10V with the furnished 10:1 dividers. The HP 11748A comes complete with all signal and power cabling. $2995.

Hewlett-Packard Co, Inquiry Handling Service Inc, 200 Parkside Dr, Account 102PR, Dept 12, San Fernando, CA 91340. Phone local sales office.

Circle No 382

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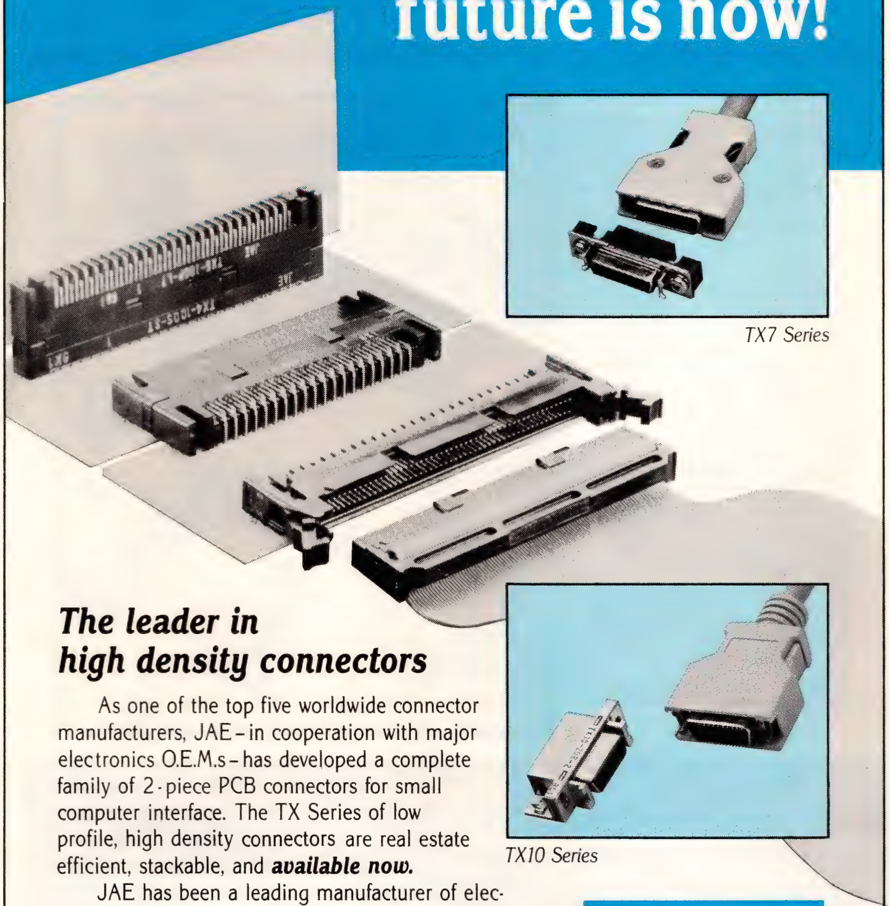

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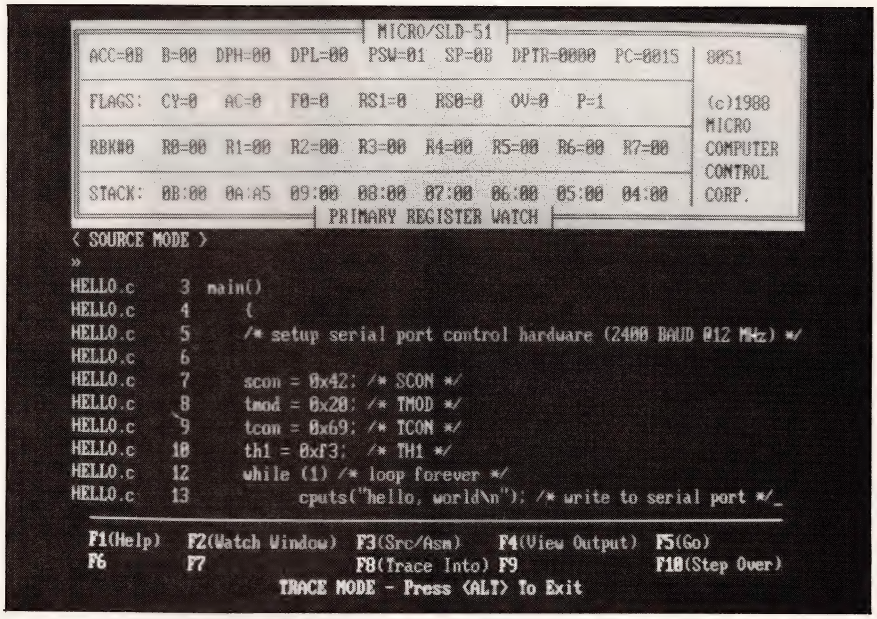
CIRCLE NO 103

CAE & SOFTWARE DEVELOPMENT TOOLS

C CROSS COMPILER

- *Lets you develop software for single-chip μCs*
- *Gives C programs access to multiple memory address spaces*

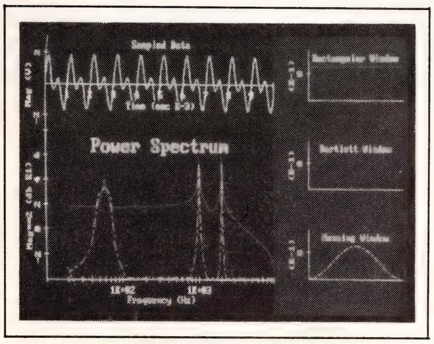
Micro/C, a C cross-compiler, runs on IBM PCs and compatibles and generates assembly-language code for 8051, Z8, or Super 8 microcontrollers. You can then use a corresponding cross-assembler to generate executable code. Standard C does not directly support interrupts, but most μCs have an elaborate interrupt structure for on-chip and off-chip devices; Micro/C's library lets you make any C function interrupt driven by prefixing the function name with the key word "interrupt." The compiler's map specifier lets you identify the memory space in which any variable in your C code resides. This feature allows fast 1- or 2-byte instructions to access variables resident in any of the multiple on-chip or off-chip memory spaces for which the system is configured—a difficult task for standard C, which relies on a single memory map. C cross-compiler, $595; cross-assembler, $295; cross-compiler/cross-assembler kit, $850.



```
                              MICRO/SLD-51
ACC=0B  B=00  DPH=00  DPL=00  PSW=01  SP=0B  DPTR=0000  PC=0015 | 8051
FLAGS:  CY=0   AC=0   F0=0   RS1=0   RS0=0   OV=0   P=1         | (c)1988
RBK#0   R0=00  R1=00  R2=00  R3=00  R4=00  R5=00  R6=00  R7=00  | MICRO
                                                                | COMPUTER
                                                                | CONTROL
STACK:  0B:00  0A:A5  09:00  08:00  07:00  06:00  05:00  04:00  | CORP.
                         PRIMARY REGISTER WATCH
< SOURCE MODE >
»
HELLO.c    3  main()
HELLO.c    4      {
HELLO.c    5      /* setup serial port control hardware (2400 BAUD @12 MHz) */
HELLO.c    6
HELLO.c    7      scon = 0x42; /* SCON */
HELLO.c    8      tmod = 0x20; /* TMOD */
HELLO.c    9      tcon = 0x69; /* TCON */
HELLO.c   10      th1 = 0xf3;  /* TH1 */
HELLO.c   12      while (1) /* loop forever */
HELLO.c   13              cputs("hello, world\n"); /* write to serial port */_
  ____________________________________________________________________
  F1(Help)  F2(Watch Window)  F3(Src/Asm)     F4(View Output)  F5(Go)
  F6        F7                F8(Trace Into) F9               F10(Step Over)
                      TRACE MODE - Press <ALT> To Exit
```

Micro Computer Control Corp, Box 275, Hopewell, NJ 08525. Phone (609) 466-1751.

Circle No 365



INTERACTIVE DSP TOOL

- *Provides independent console and graphics windows*
- *Lets you link independent processing files*

PC Data Master 2.0 is an interactive DSP (digital signal processing) and analysis package that runs on IBM PCs, PS/2s, and compatibles. The shell provides independent console and graphics windows, as well as piping facilities that let you link independent executable (.EXE) files to perform multistage data transformations. The graphics module allows you to display waveforms derived from individual or multiple data files. You have full control over colors, titles, labels, and other display parameters, and you can store display-design templates in disk files for subsequent use. The DSP utilities have been greatly augmented in Version 2.0 and include fundamental operations such as forward and inverse FFT and FHT (Fast Hartley Transform) routines, convolution, correlation, filter design, and test-data generation facilities. The package also provides data-acquisition routines for use with MetraByte's Dash-08 and Dash-16 analog input boards. The program is menu driven and has extensive on-line help facilities. To run the program, you need an IBM PC/XT, PC/AT, PS/2, or compatible with at least 256k bytes of RAM; two 360k-byte floppy-disk drives; and a CGA, Hercules, EGA, or VGA graphics card with an appropriate monitor. A hard disk and a math coprocessor enhance the program's performance but are not mandatory. $135; demo disk, $10.

Durham Technical Images, Box 72, Durham, NH 03824. Phone (603) 868-5774.

Circle No 366

LAYOUT CAD

- *Produces wiring schedules for wire-wrapped prototyping boards*
- *Lets you use generated netlist as a basis for pc-board layouts*

Running on IBM PCs or compatibles, the Netsorter router lets you optimally route wire-wrapped prototyping boards. Based on your design, the package generates a netlist that optimizes component interconnections to avoid wiring tangles and missed connections. You can

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CIRCLE NO 3
See CAPS at ELECTRO '89 Booth 2454

use the netlist as a guide when wiring boards by hand, or you can submit it to the company for use on their semiautomatic wiring machines. Once you've tested your design, you can input the netlist to standard pc-board layout packages, including Racal Redcad and Cadstar. After you enter the component pin numbers with their associated signal names, the package sorts the data and produces a wiring schedule. To eliminate cross-connected signal paths, the software flags any pins for which you define multiple signal names. In addition, the program maintains a maximum of two connections per post, allowing you to use low-profile, wire-wrap boards. The package can also produce documentation to assist in tracing signals on the board. £350.

C E Automation Ltd, Unit 15, Suttons Industrial Park, London Rd, Earley, Reading, Berkshire RG6 1AZ, UK. Phone (0734) 669414. TLX 849286.

Circle No 367

TRANSLATOR

- *Converts AutoCAD files to Gerber format*
- *Lets you edit Gerber files*

The bidirectional-translator utility program #SU-06 translates AutoCAD .DFX files to Gerber RS-274D format and vice versa. The utility also allows you to edit either Gerber RS-274D or AutoCAD .DFX files without the need for CAD or AutoCAD equipment. The utility suits applications such as pc-board and hybrid-circuit layout generation, silkscreen plotting, and desktop publishing. The program runs on IBM PCs and compatibles and requires a CGA, EGA, or VGA; a hard disk is recommended but is not mandatory. $595.

Consultek Software Systems Inc, 1400 Coleman Ave, Suite C25/26, Santa Clara, CA 95050. Phone (408) 988-8091. FAX 408-943-0589.

Circle No 368

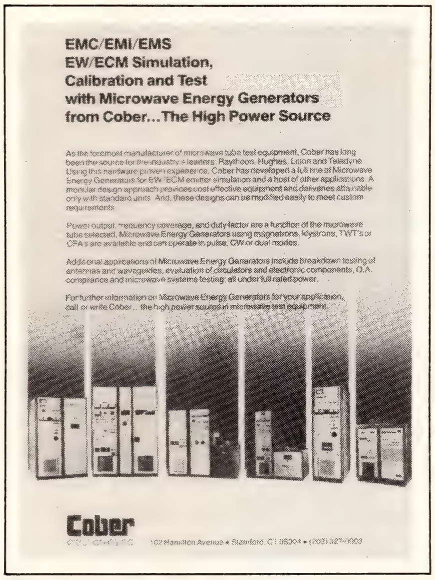
ASIC DESIGN TOOLS

- *Let you import custom-designed cells*
- *Give access to the layout in GDS or CIF formats*

ChipCrafter/AX and ChipCrafter/ICX are ASIC-design tools that use expert-system techniques to incorporate custom modules into an ASIC designed with the aid of a fully automated proprietary design tool. Until now, bringing custom modules into an ASIC system has been difficult because the foreign block is rarely compatible with the standard ASIC-simulation system. ChipCrafter/AX provides menus that let you define the layer assignments and port locations of your custom module, a simulation model of the module, and a schematic symbol in the workstation's format. The vendor's ChipCrafter ASIC-design workstation will then be able to compile the module as a block of standard cells or as an arbitrarily sized block. The large number of rulesets include a wide variety of CMOS fabrication options such as 1.0-µm features and RAD-hard capabilities. ChipCrafter/ICX provides all the features of ChipCrafter/AX, and provides tools and utilities that allow you to export all or part of a design to another design system. Because you have access to the layout in GDS or CIF formats, you can complete design-rule checking, electrical-rule checking, and layout-vs-schematic verification at the design site, and then take the design to any qualified foundry for fabrication. Both tools come with an automatic interface to Mentor Graphics (Beaverton, OR) IDEA workstations. ChipCrafter/AX, $108,000; ChipCrafter/ICX, $149,000.

Seattle Silicon Corp, 3075 112th Ave NE, Bellevue, WA 98004. Phone (206) 828-4422. FAX 206-827-4224.

Circle No 369



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Brochure on microwave energy generators

This brochure describes the vendor's full line of high-power microwave energy generators for EW/ECM (electronic wave/electronic countermeasure) emitter simulation. The publication discusses how the generators are used in testing electromagnetic compatibility, EMI, and electromagnetic susceptibility, as well as breakdown testing of antennas and waveguides and evaluation of circulators and electronic components.

Cober Electronics Inc, 102 Hamilton Ave, Stamford, CT 06902.

Circle No 420

Troubleshooting metastable events

Locating and eliminating component failures caused by random transitions in logic levels is the subject of the vendor's application note, *Troubleshooting Metastable Events Using the Gated Totalize Counter Feature of the Tektronix 11300A Series Oscilloscope (47W-7008).* Targeted at people who perform component testing, digital design, and computer peripheral testing, the note explains how to make use of the 11300A Series oscilloscope's writing speed, 750-MHz counter/timer, and oscilloscope functions. Also included are step-by-step instructions on how to set up the oscilloscope and tips on the best way to probe the circuit under test.

Tektronix Inc, Box 1700, Beaverton, OR 97077.

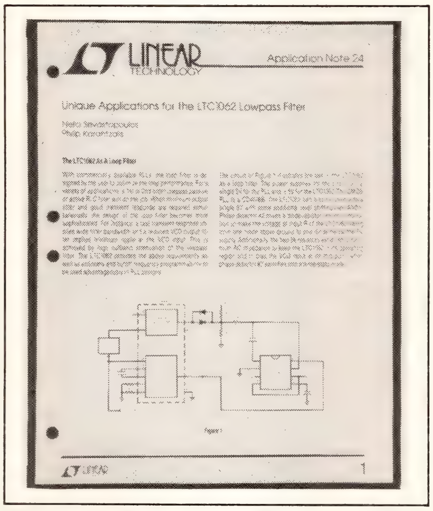
Circle No 421

Guide to IEEE-488.2 command interface

The vendor's application note, *Getting Started With IEEE-488.2,* presents this IEEE-488.1-standard extension, which focuses on the software aspects of automated systems. The note is principally intended to support the company's 1281 Selfcal DMM, one of the first instruments to incorporate the IEEE-488.2 command and message-exchange interface. The guide is expected to be of primary interest to users who are already familiar with IEEE-488 (1978) systems.

Datron Instruments, Wavetek Corp, Box 85434, San Diego, CA 92138.

Circle No 422



LINEAR TECHNOLOGY
Application Note 24

Unique Applications for the LTC1062 Lowpass Filter

Nello Sevastopoulos
Philip Karantzalis

The LTC1062 As A Loop Filter

Figure 1

1

Using a lowpass filter as a loop filter

AN 24: Unique Applications for the LTC1062 Lowpass Filter explains how to use the vendor's lowpass filter as a loop filter, providing minimum output jitter and good transient response. The note includes the design for a clock-sweepable pseudo-bandpass/notch filter and discusses schematics and component values. Further, the publication advises you on cascading the devices for higher precision, accommodating high-input voltages, and programming filters for a wide variety of cutoff frequencies.

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035.

Circle No 423

Abridged catalog lists hardware and software products

The 6-pg short-form version of the vendor's product catalog describes IEEE-488 bus interfaces for IBM PCs and compatible computers and Apple Macintosh personal computers. The 4-color publication presents specifications and prices for 33 hardware and software products. It also provides a list of sales and support contacts and supplemental descriptions of the products listed in the brochure.

IOtech Inc, 25971 Cannon Rd, Cleveland, OH 44146.

Circle No 424

Bulletin introduces EPROM programmer

The company's Product Bulletin No P-1287 depicts the Model 7128 EPROM programmer as a high-performance device equipped with microprocessor-based intelligence for ease of use and interface. The bulletin highlights two useful features of the programmer: the compare mode, which allows you to compare source files with programmed devices, and the algorithm-only feature, which programs cells that are different from the source code. A specification table, a list of commands, and an explanation of diagnostic error codes round out the bulletin.

Entertron Industries Inc, 3857 Orangeport Rd, Gasport, NY 14067.

Circle No 425

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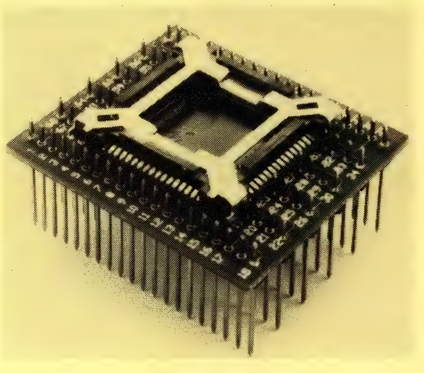

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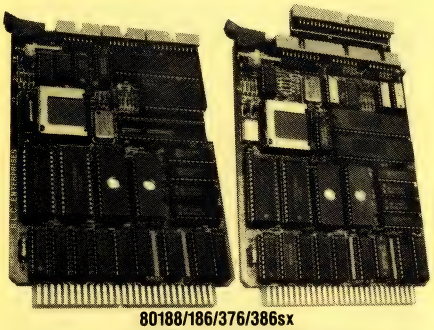

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CIRCLE NO 328

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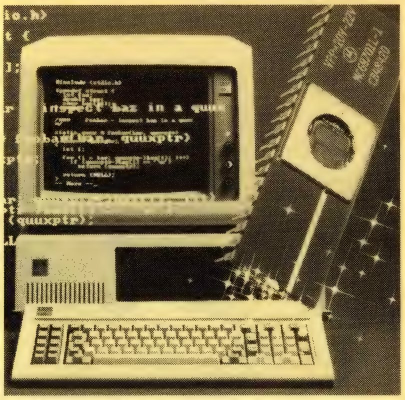

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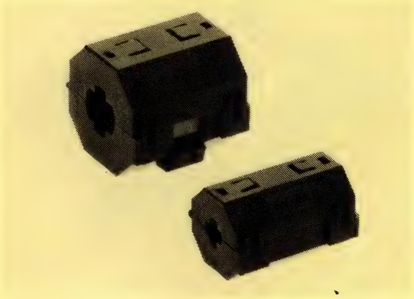

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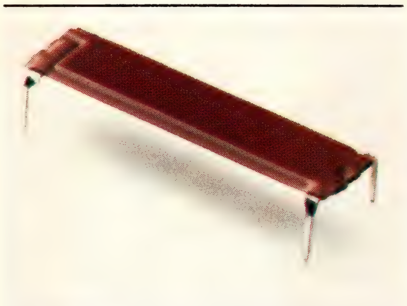

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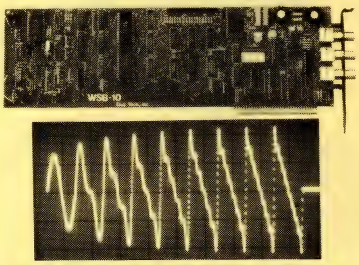

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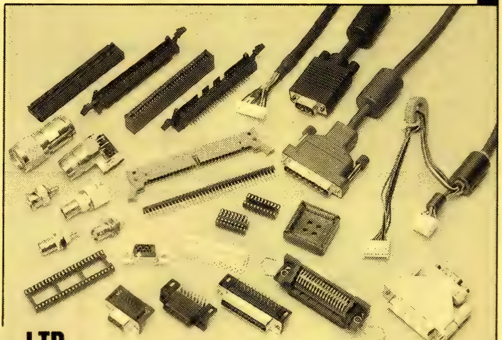

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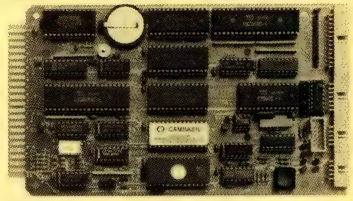

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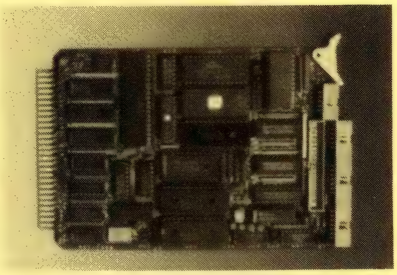

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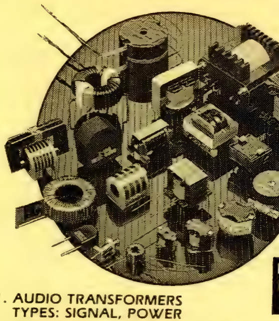

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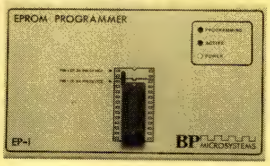

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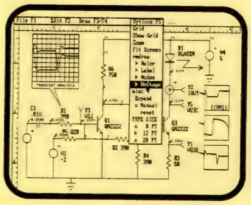

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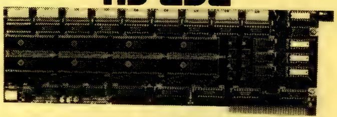

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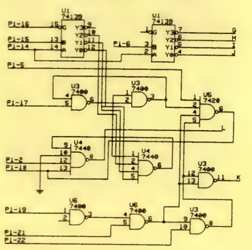

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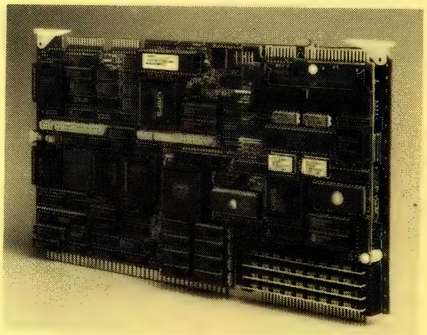

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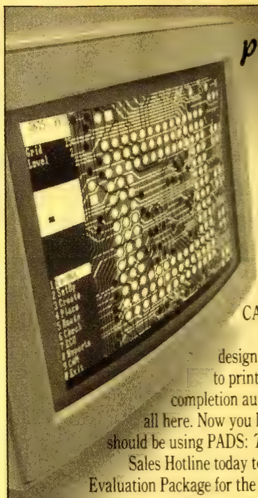

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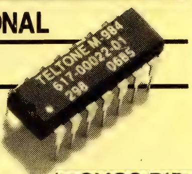

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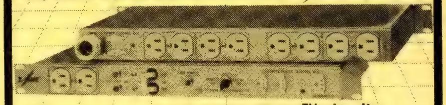

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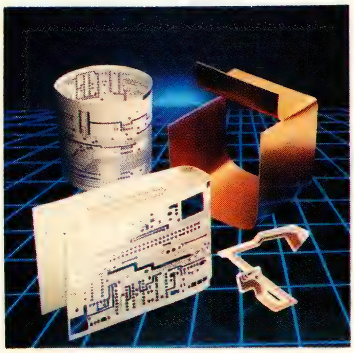

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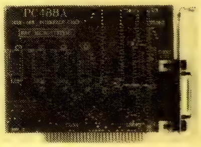

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Mar. 30	Mar. 9	Integrated Circuits, Computer Boards	Closing: Mar. 17 Mailing: Apr. 6
Apr. 13	Mar. 23	Test & Measurement, Digital ICs	Closing: Mar. 31 Mailing: Apr. 20
Apr. 27	Apr. 6	Communications Technology, Special Issue Communication ICs	Closing: Apr. 13 Mailing: May 4
May 11	Apr. 20	Analog Technology, Special Issue Computer Peripherals	Closing: Apr. 28 Mailing: May 18
May 25	May 4	Digital ICs, Computer Peripherals	Closing: May 25 Mailing: June 15
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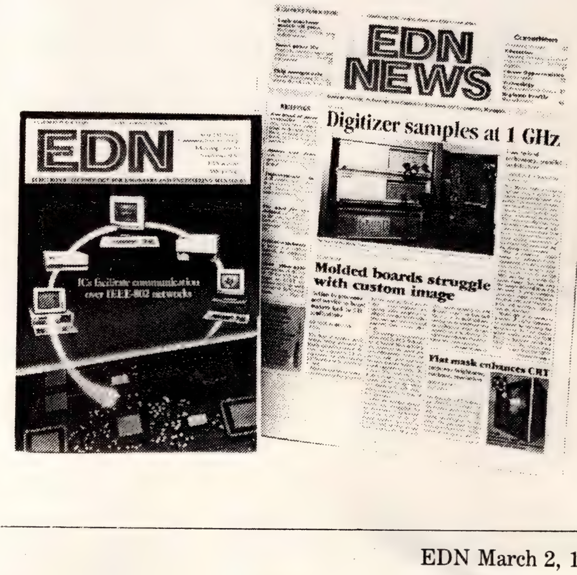

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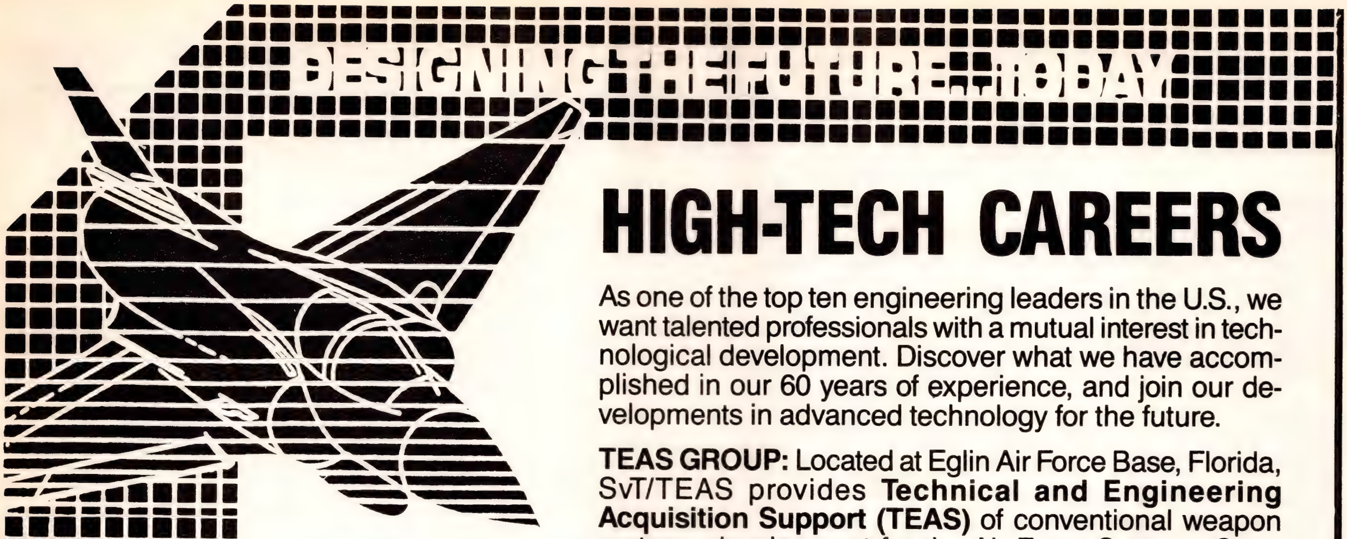

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Peter D Coley
VP/Publisher
Newton, MA 02158
(617) 964-3030; Telex 940573
Ora Dunbar, Assistant/Sales Coordinator

Mark J Holdreith
Advertising Sales Director
Newton, MA 02158
(617) 964-3030
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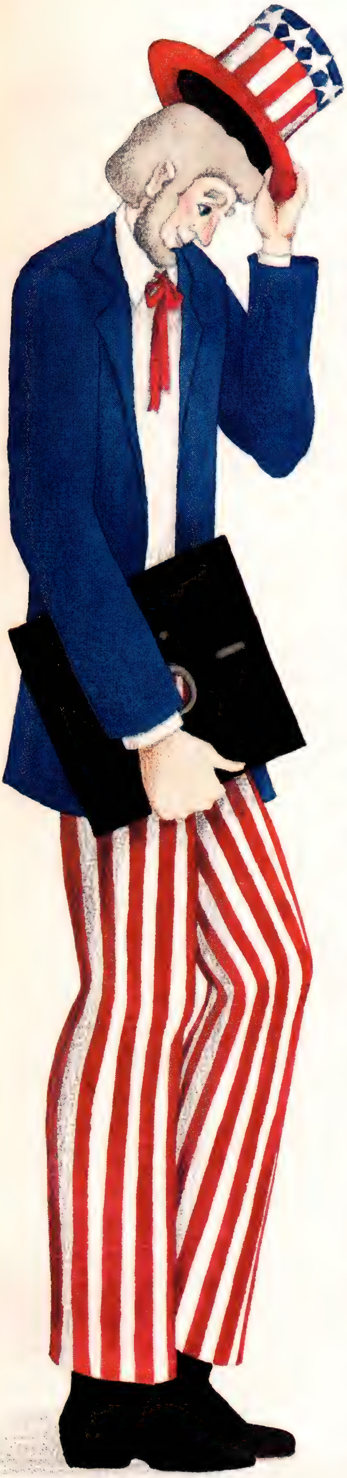
Private developer vs federal government: Retaining software rights requires vigilance

Stephen T Owen

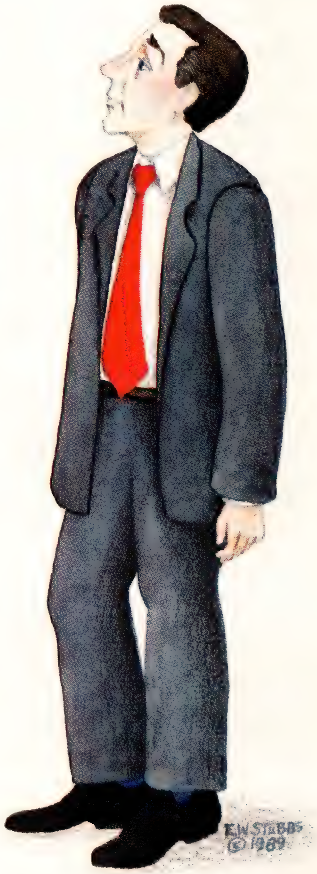


Elizabeth Stubbs

By anyone's standard, the federal government is a major purchaser of computer hardware, software, and services. Estimates of annual expenditures vary, but a figure in the tens of billions of dollars isn't far wrong. And of course this amount will continue to increase. A substantial portion of these expenditures goes toward the acquisition of software packages to aid in innumerable computerized and computer-assisted governmental functions—from routine book- and recordkeeping and management tasks to highly sophisticated space, intelligence, and military operations. The General Services Administration estimates that the government will have approximately one-half million microcomputers by 1990, accompanied by vast demands for software. Designers, programmers, and vendors of computer software have to find the answer to a vexing question: How to apportion proprietary rights between the federal customer and the private seller.

It is hardly surprising that when the government pays the full cost of developing software for a unique government application, the government acquires all proprietary interest in the software—not only the right to use it, but also the right to copy, license, or resell it. The vendor retains no interest. In many cases, however, the software is a product of private commercial enterprise using entirely private funding. The software may very well have valuable commercial as well as governmental applications; understandably, the vendor wants to retain complete proprietary interest. In this scenario, the government is just one customer among many.

The issue becomes complicated when the software is developed with a mixture of public and private funds. Say, for example, that a private entrepreneur develops a program as a general concept, and the government then pays for final development for a specific application. Another complication arises when a private company develops a complete software package with private funds, and the government subsequently pays for a particular modification of the package for a specific federal function or activity.



The government does, of course, claim title to certain rights if it has invested public funds in a software package. Where to draw the line is difficult to ascertain. According to some interpretations of the regulations, the government can claim unlimited rights to software even if the expenditure is a relatively modest one; if, for instance, the features developed at private expense are not readily distinguishable from the modifications incorporated at government expense.

No matter what the arrangement, a vendor must be diligent—and prudent—and protect its legitimate proprietary interests. Above all, you must avoid the risk of forfeiting those interests or of giving the government greater rights than originally intended. This advice holds true during negotiations with the government as well as afterwards, when it comes time to fulfill the contract.

Regulations covering the government's acquisition of automatic data-processing software (and related standard-contract clauses) have been in a continual state of flux in recent years. This is particularly true in the defense area. Congress and the defense purchasing agencies are attempting to create a workable balance between the interests of the government in acquiring rights to software it purchases and the interests of private enterprise in retaining valuable proprietary rights of software that it has developed. Congress has acknowledged that many times it is important for the government to obtain unlimited rights to software, but that nonetheless the government must provide incentives to private industry. The private sector needs motivation to independently develop technologies that defense and other government activities require; to do so, the private sector needs to retain full exploitation rights to those technologies—consistent with the government's interest, of course.

The initial effort to refine the regulations began several years ago. Congress became concerned that procuring agencies, and the Department of Defense (DoD) in particular, were too lax in acquiring rights to software and technical data that the govenment had provided developmental funding for. Congress perceived this lack of diligence as the reason why the government was paying premium prices to sole-source vendors. They viewed this practice as limiting competition and the development of alternate sources of supply, which is important for defense mobilization.

At this time, Congress directed the DoD to expedite new regulations to ensure greater protection of the government's interests while still giving due protection to private proprietary rights. Simultaneously, Congress directed the Office of Federal Procurement Policy (the unit within the Office of Management and Budget having oversight responsibility for federal acquisition regulations) to develop government-wide regulations in conjunction with the DoD and civilian agencies.

Interim DoD regulations became effective in April 1988, but many inside and outside of government viewed them as excessively restrictive and one-sided. Among other things, the regulations created situations in which private proprietary rights were inadvertently forfeited; gave rise to the presumption that in mixed-funding projects the government received unlimited rights; and failed to give due recognition to subcontractors' rights. Accordingly, under Congressional prodding, the DoD published a substantially revised interim rule, which governs solicitations and resulting contracts issued after October 31, 1988.

The Office of Federal Procurement Policy has stated that the development of any new government-wide regulations will await further study and refinement of the DoD regulations. The office intends to model the new regulations on the DoD regulations with suitable modifications that take into account the civilian agencies' different requirements.

In reviewing the applicable regulations and contract clauses, you must remember to carefully distinguish between those pertaining to "computer software" and those pertaining to "technical data." Although the same section of the regulations covers both subjects, you'll find that each receives significantly different treatment.

The regulations broadly define technical data as "recorded information, regardless of the form or method of recording, of a scientific or technical nature (including computer software documentation)."

The definition does not, however, "include computer software . . . ."

The term "computer software" embraces "computer programs and computer databases." A computer program is "a series of instructions or statements in a form acceptable to a computer, designed to cause the computer to execute an operation or operations," whereas a computer database is "a collection of data in a form capable of being processed and operated on by a computer." Computer programs expressly include operating systems, assemblers, compilers, interpreters, data-management systems, utility programs, sort-merge programs, and automatic data-processing equipment maintenance and diagnostic programs, as well as applications programs such as payroll, inventory control, and engineering analysis.

As mentioned earlier, the ownership issue is more or less straightforward when the software is developed (that is, brought to the point of being workable) "exclusively with government funds"; the government generally obtains "unlimited rights" to the software and any related technical data. Unlimited rights means the right to use, duplicate, release, or disclose information about the software, and to permit others to do so. The government may, for example, contract with the vendor's competitors to reproduce any software that it holds according to unlimited rights.

On the other hand, when the government acquires software that was developed exclusively with private funds, the government acquires only "restricted rights": the right to use the software with the computer for which it was designed (or backup computers as appropriate) and the right to copy it for archival purposes. The government can also modify the restricted-rights software or merge it with other software, but the restricted-rights protection still applies to the restricted rights' portion of the software.

The regulations stipulate that other rights that the government might acquire with "restricted rights" software are subject to appropriate licensing agreements. Any such agreement should carefully define the government's obligation not to disclose information about the software if such a disclosure could have an adverse competitive impact on the vendor.

The guidelines are less clear regarding software developed with a combination of private and government funding. The fault lies partly with the regulations on technical data, which permit the government to accept "government-purpose license rights," that is, the right to use the data for any government purpose while leaving all commercial rights with the vendor. There is no equivalent provision for computer software.

When software that was developed at private expense is modified or enhanced as a necessary part of performing a government contract, "only that portion of the resulting product in which the original product is recognizable will be deemed to be computer software developed at private expense to which restricted rights may apply." This provision makes it imperative that a software designer or programmer use special care when modifying proprietary software items for government use. The developer should always strive to devise a way to achieve the desired tasks in such a way that the original product is preserved in recognizable form as much as possible.

In all other cases, the regulations and related standard-contract clauses suggest negotiated resolutions of mixed-funding problems. It is most important for vendors to note that the burden is on the vendor to notify the government of its intent (or a subcontractor's intent) to use software developed partly at government and partly at private expense to fulfill a contract. You should notify the government before the contract is awarded, if possible, and before the software is actually used, in any case.

The regulations clearly suggest that the government negotiate in good faith, not acquire greater rights to either software or data than is required to meet its legitimate needs, encourage commercialization by the contractor of products that the government purchases (to reduce overall costs), and encourage private innovation by strictly respecting the contractor's legitimate proprietary rights.

Nonetheless, vendors should not expect purchasing agencies to recognize, without any guidance from the contractor, how rights should be apportioned. Be forewarned that government officials look askance at late-arising assertions of proprietary rights. If issues pertinent to the apportionment of the proprietary rights are not resolved prior to the award of a contract, the government's contracting officer has

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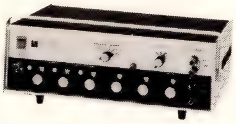

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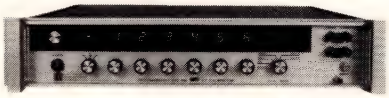

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the right to make a unilateral determination as to apportionment, leaving only a disgruntled vendor. Although a vendor has rights under the Dispute Clause, resolving a unilateral determination may ultimately involve extensive proceedings before a federal court or contract appeals board, can be costly and protracted, and carry the usual risks inherent in any litigation.

For software designers and vendors seeking to do business with the government, the keynote is early identification of potential issues. Also, the contractor needs to identify the items or components for which he wants to retain property rights. In most cases, you are well advised to draw up a license agreement that clearly delineates the respective rights of the vendor and the government. The scope of the agreement should include restricted rights, confidentiality, and identification of mixed-funding software; associated documentation and other data should be carefully marked with appropriate restrictive legends prior to delivery.

The regulations broadly define technical data as "recorded information, regardless of the form or method of recording, of a scientific or technical nature (including computer software documentation)."

At all times—not just during negotiations—the contractor should be prepared to justify claims of proprietary rights. The government's right to challenge restrictions on the use of computer software and technical data survives the award of a contract and even completion of the contract. Meticulous keeping of historical records and pertinent correspondence is essential. Accuracy in negotiations is also important to avoid civil and criminal liability for fraud or false claims. A contractor should coordinate proprietary concerns with subcontractors because the burden of dealing with the government is primarily the responsibility of the prime contractor. Prime contractors should realize that the new regulations protect a subcontractor's rights and prohibit higher-tier contractors from using their economic leverage to force subcontractors to surrender proprietary rights.

Don't be misled and think that charting a course through the contract negotiation process is simple. The government has so far been unable to firmly define its objectives respecting software rights. Further rulemaking lies ahead. It is, therefore, all the more indispensable for the contractor or vendor to clearly define in advance its own objectives regarding proprietary rights and to be persistent through the negotiation process. A lack of diligence can be costly: The ability of government contracting officials to waive or deviate from the regulations is actually very limited. **EDN**

Stephen T Owen is a partner in the Washington, DC, law firm of Kominers, Fort & Schlefer and specializes in federal procurement law.

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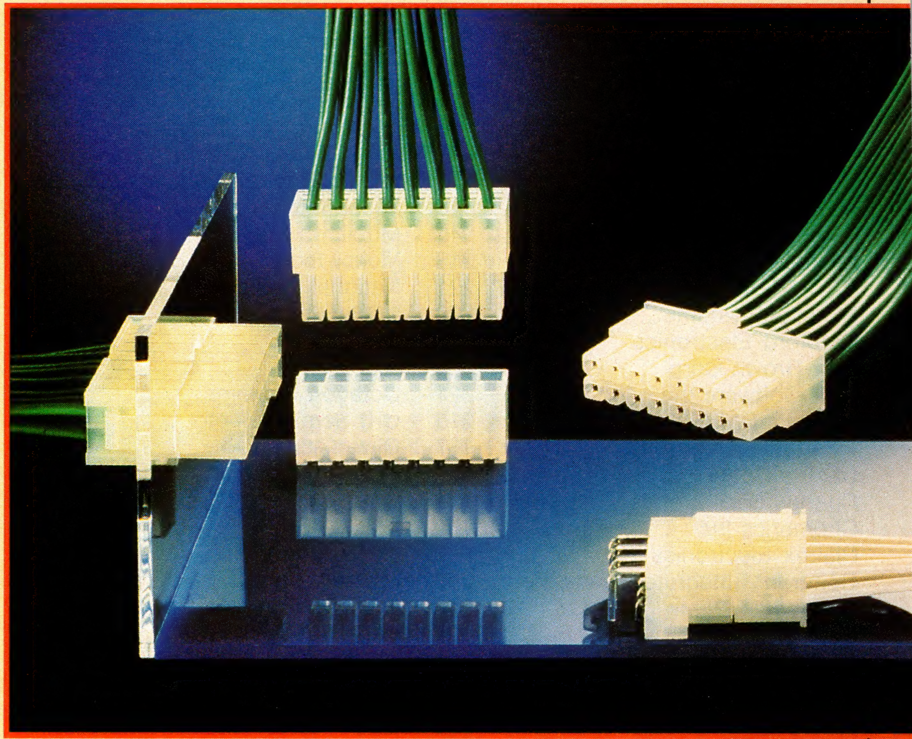

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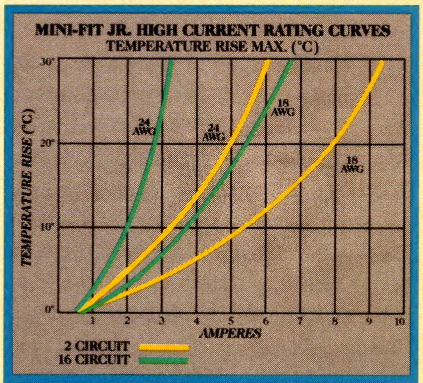

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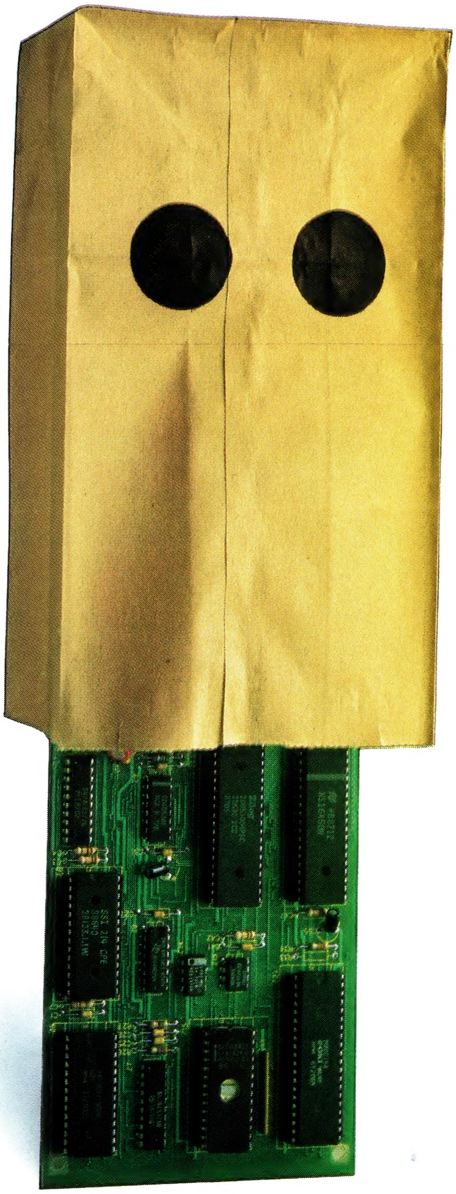

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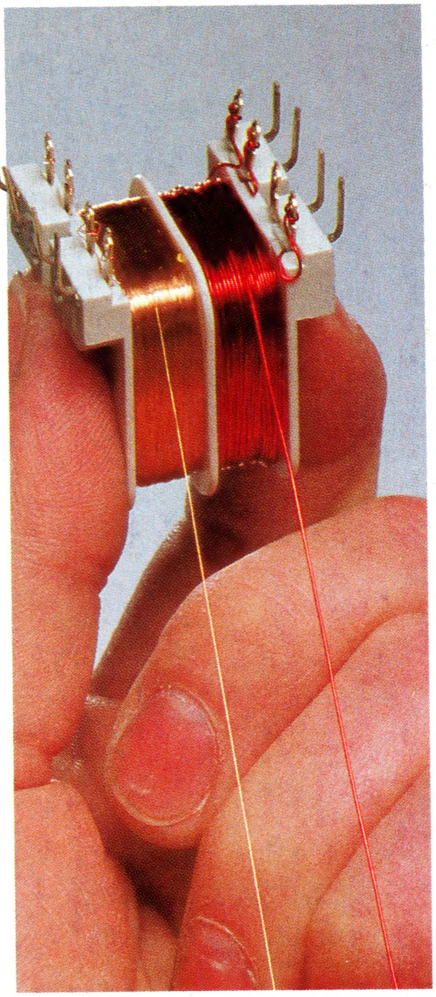

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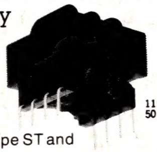

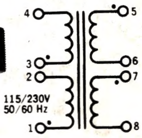

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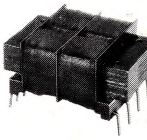

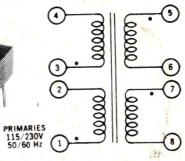

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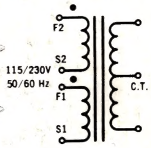

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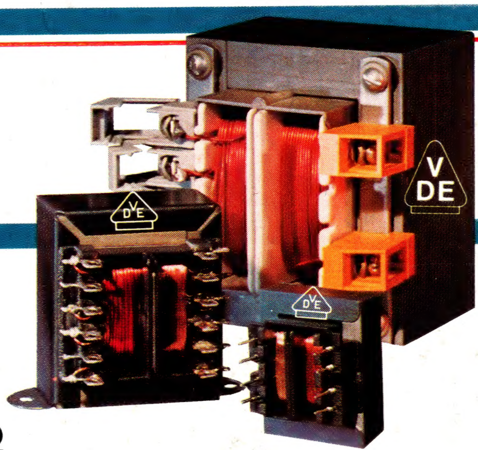

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